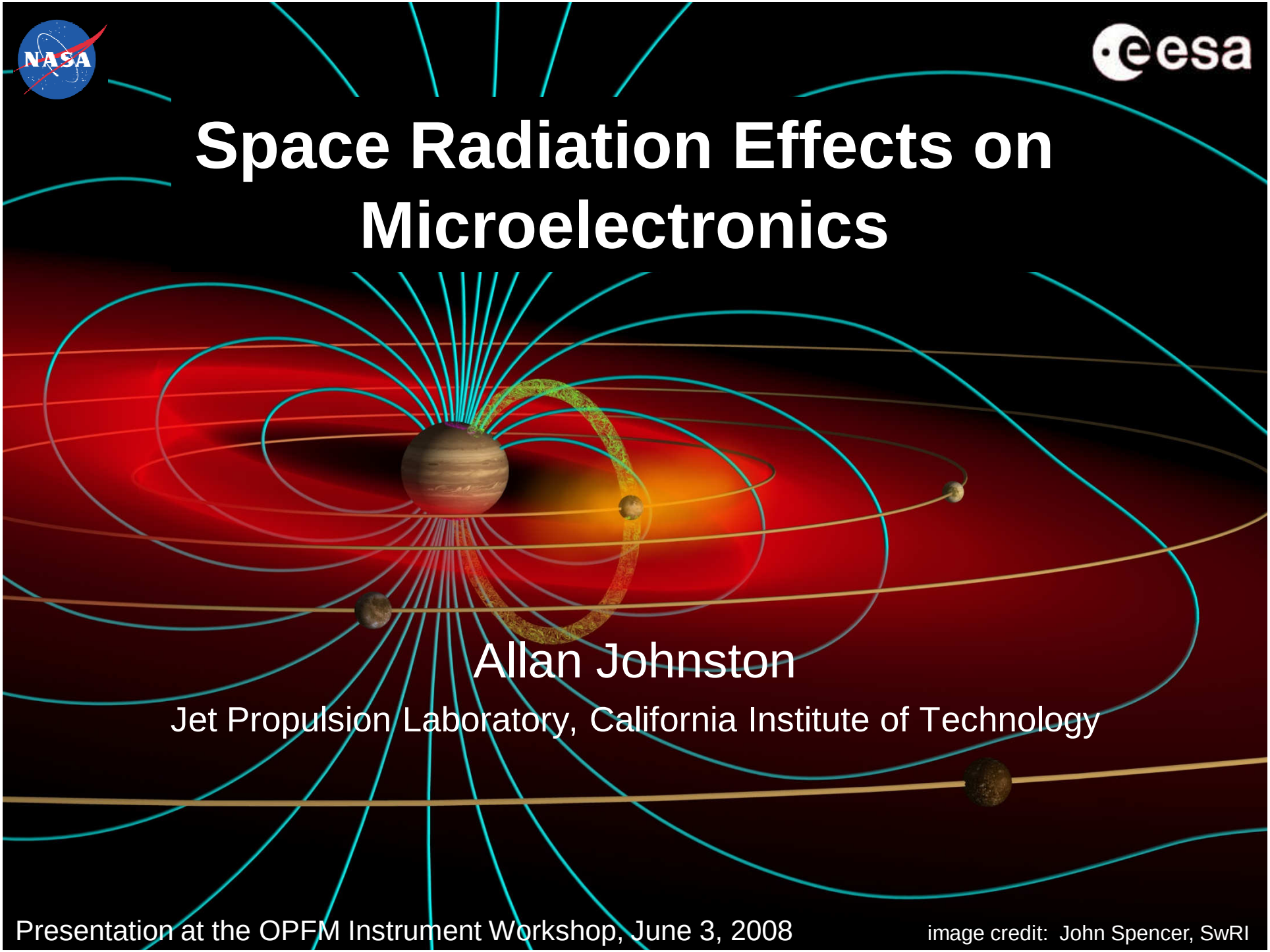


Space Radiation Effects on Microelectronics

Allan Johnston

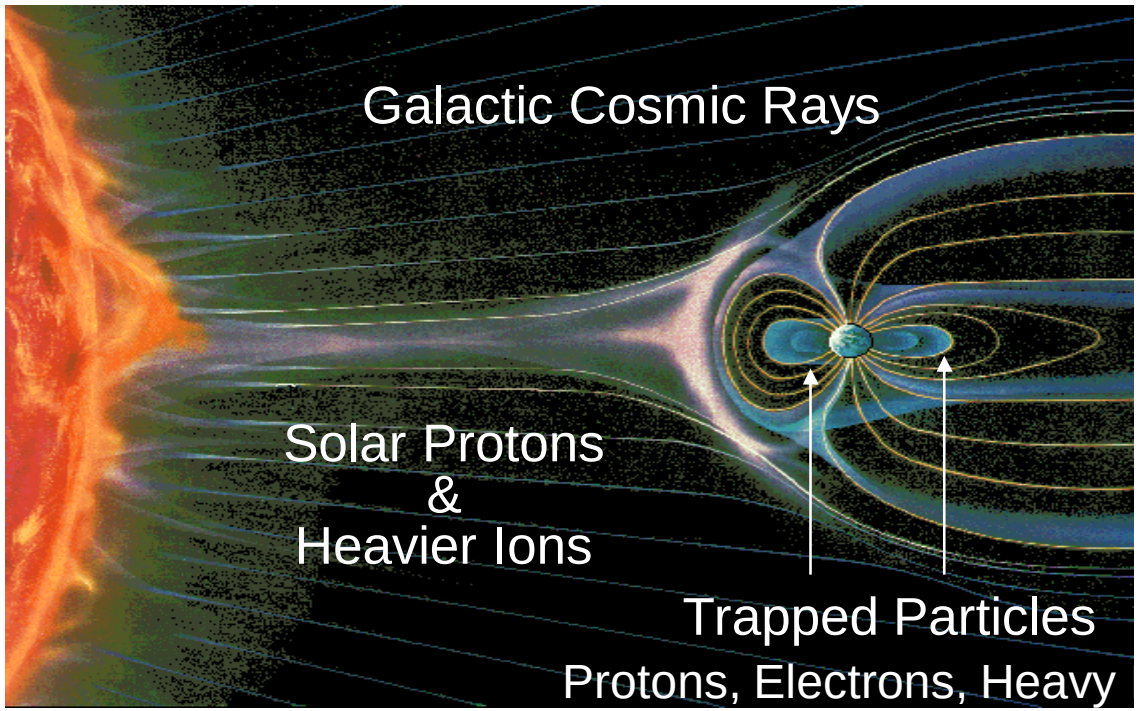
Jet Propulsion Laboratory, California Institute of Technology

Presentation at the OPFM Instrument Workshop, June 3, 2008

image credit: John Spencer, SwRI

Introduction

- Galactic cosmic rays occur everywhere in space
- Solar particles and the earth's trapped radiation belts affect the space radiation environment near the earth. More intense trapped belts occur at Jupiter.



Nikkei Science, Inc. of Japan, by K. Endo

Distinctions between Fundamental Mechanisms

Integrated effects of many particle interactions

- Charge trapping effects (total dose damage)
- Bulk damage (atoms are displaced, decreasing minority carrier lifetime)

The high total dose levels are the distinguishing feature of the Europa mission

Effects from a single energetic particle

- Generates small, spurious charge pulses within electronics
- Can produce transient and permanent effects
- First noted in 1975 in operating spacecraft, and has become increasingly important as devices have evolved

D. Binder, E. Smith and A. Holman, IEEE Trans. Nucl. Sci., p. 2675, Dec. 1975

Outline

- Space Radiation Environment I: *Integrated damage effects*
- Total Dose Damage
  - MOS transistors and CMOS
  - Bipolar devices
- Displacement Damage
  - Lifetime damage
  - Displacement damage in linear integrated circuits
  - Displacement damage in optoelectronic devices
- Summary and Conclusions

Ionization: Production of Electron-Hole Pairs

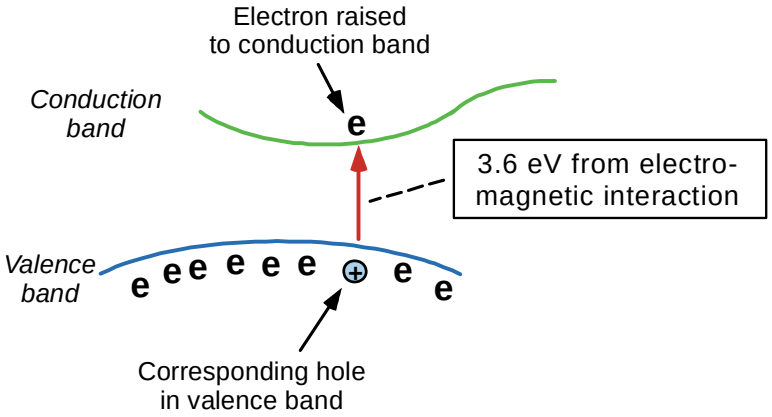
Total dose (absorbed dose), is measured in rads

1 rad = 100 erg per gram of material

Energy to create an e-h pair:

~ 3.6 eV in silicon

~ 18 eV in silicon dioxide



The net effect depends on how the excess charge is rearranged before coming to equilibrium

- Electrons are mobile, and migrate quickly to interface regions
- Holes migrate much more slowly, in the opposite direction of electric fields that are present in the insulator
- Traps form at interface regions after hole migration, which is the most important mechanism for total dose damage

Environment

Trapped Radiation Belts – *a steady source of radiation*

- LEO orbit (300 to 1400 km): protons in the South Atlantic Anomaly
- MEO orbit (1400 to 4000 km): protons in the trapped belt
- Geosynchronous orbit: electrons in the outer trapped radiation belt
- Jovian belts: high-energy electrons with very high total dose levels

Solar Flares – *an erratic radiation environment*

- LEO orbit
- Geosynchronous orbit (and deep space)
- Depends on the probability of encountering large solar flares

For Europa we can ignore the total dose component of solar flares (except for peak flux) because the total dose level in the jovian belts is so high

Typical Total Dose Levels for Various Orbits and Missions [surface dose per year]

Earth (*nearly all from trapped particles*)

– LEO (ISS - Shuttle)	~ 2 krad (protons)
– MEO	~ 100 krad (protons and electrons)
– GEO (GOES)	~ 10 krad (electrons)
– Transfer (CRRES)	~ 50 krad (protons and electrons)

Mars (*all from flares*)

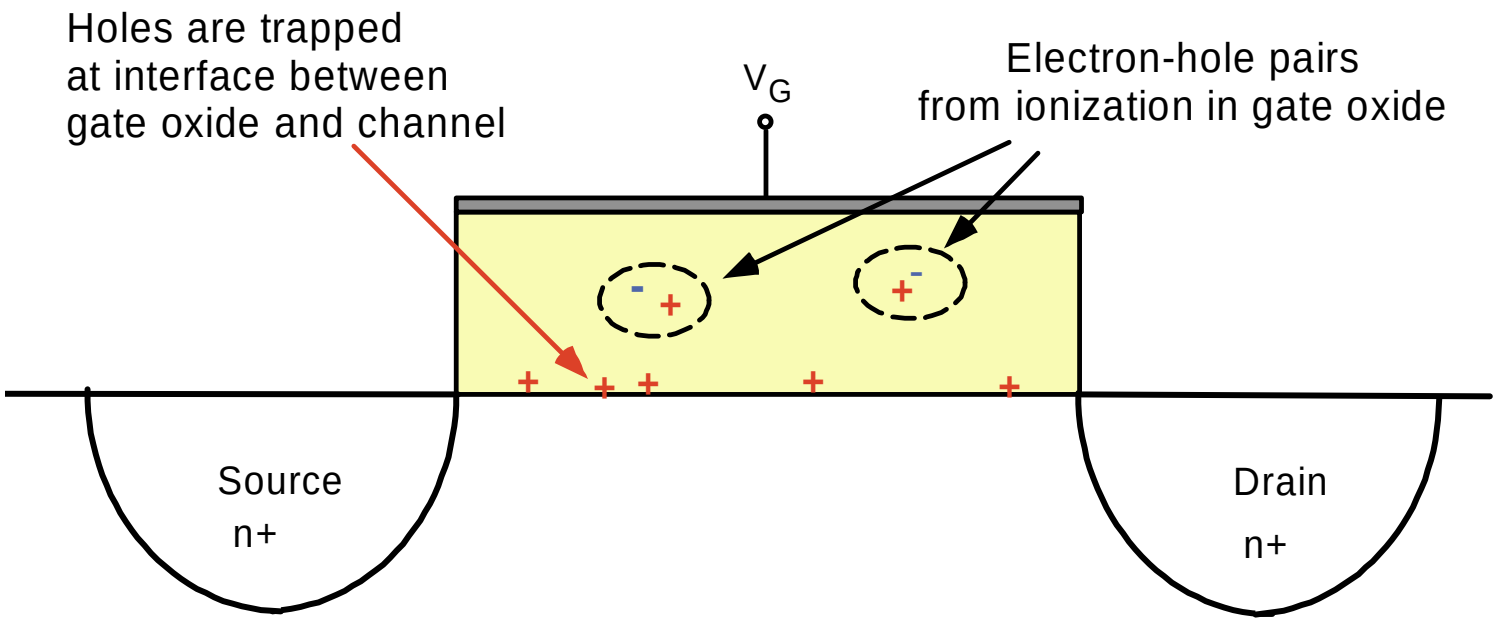
– Surface	~ <1 krad (heavy particles)
– Orbit	~ 5 krad (protons)
– Transit	~ 5 krad (protons)

Jovian

– Exploration orbits	~ 100 krad –100 Mrad (electrons and protons)

Jovian missions have extremely high radiation levels

Total Dose Effects in MOS Gate Oxides



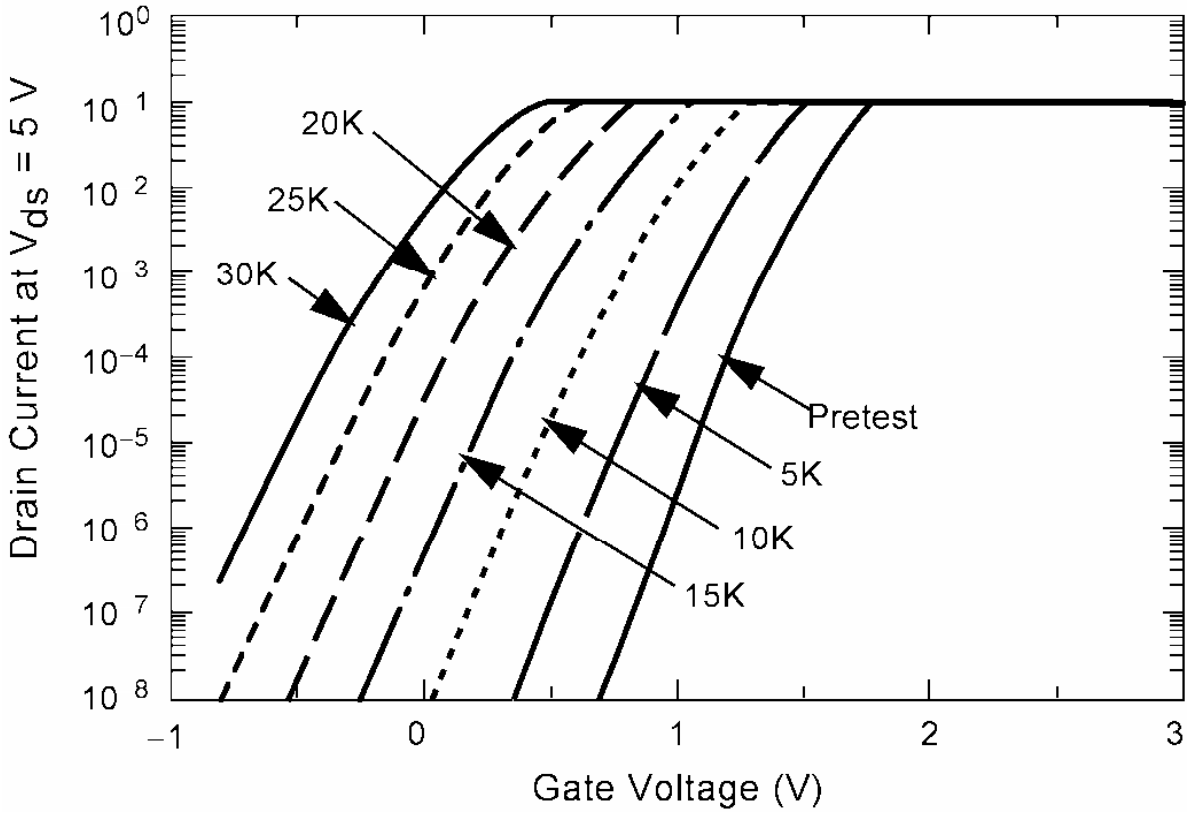
Ionization produces electron-hole pairs within the gate

Holes are trapped at oxide-silicon interface

- Changes gate threshold voltage
- Two types of traps: hole traps and interface traps

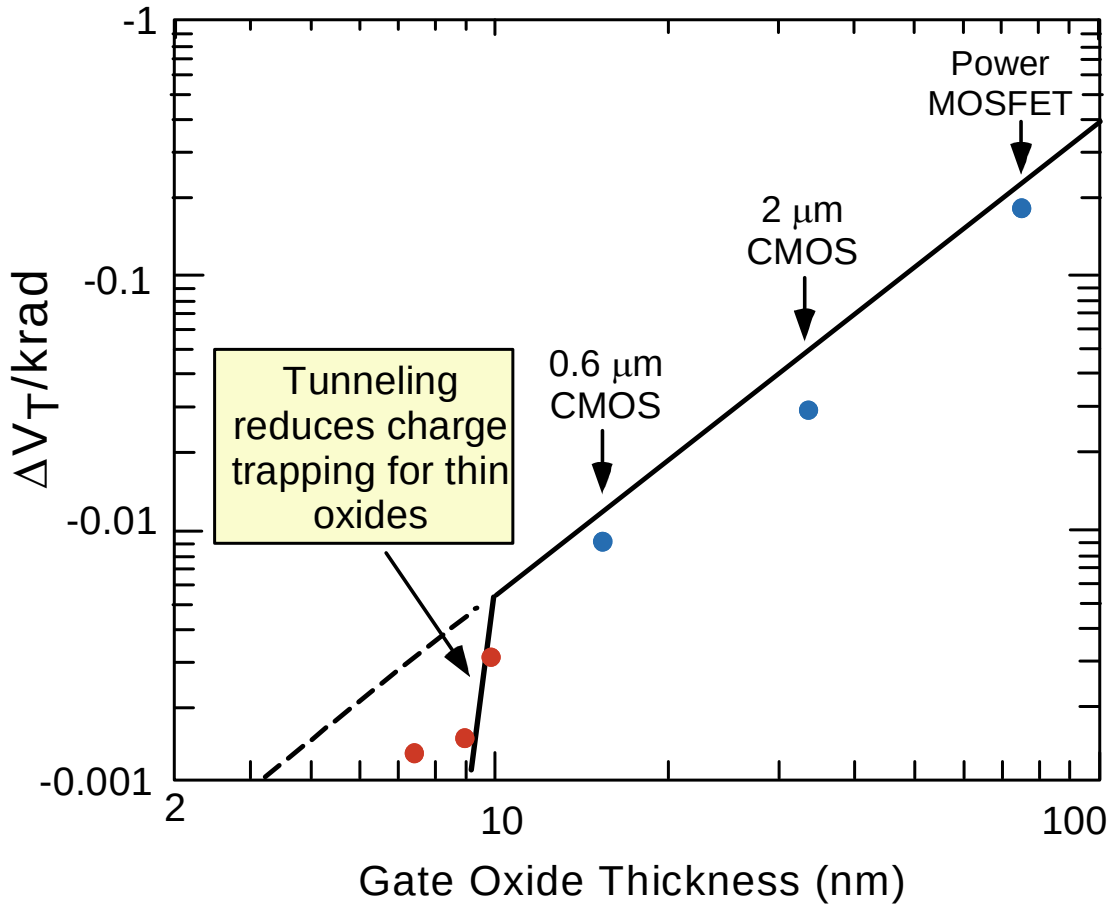
Threshold Shift in NMOS Transistors with Thick Gate Oxides

Ionization damage causes a negative shift in gate threshold voltage, eventually preventing the device from turning “off” unless a negative gate voltage is applied



Oxide Trapping Depends on the Oxide Thickness

Scaling has reduced total dose damage in the thin gates that are typical of modern processes

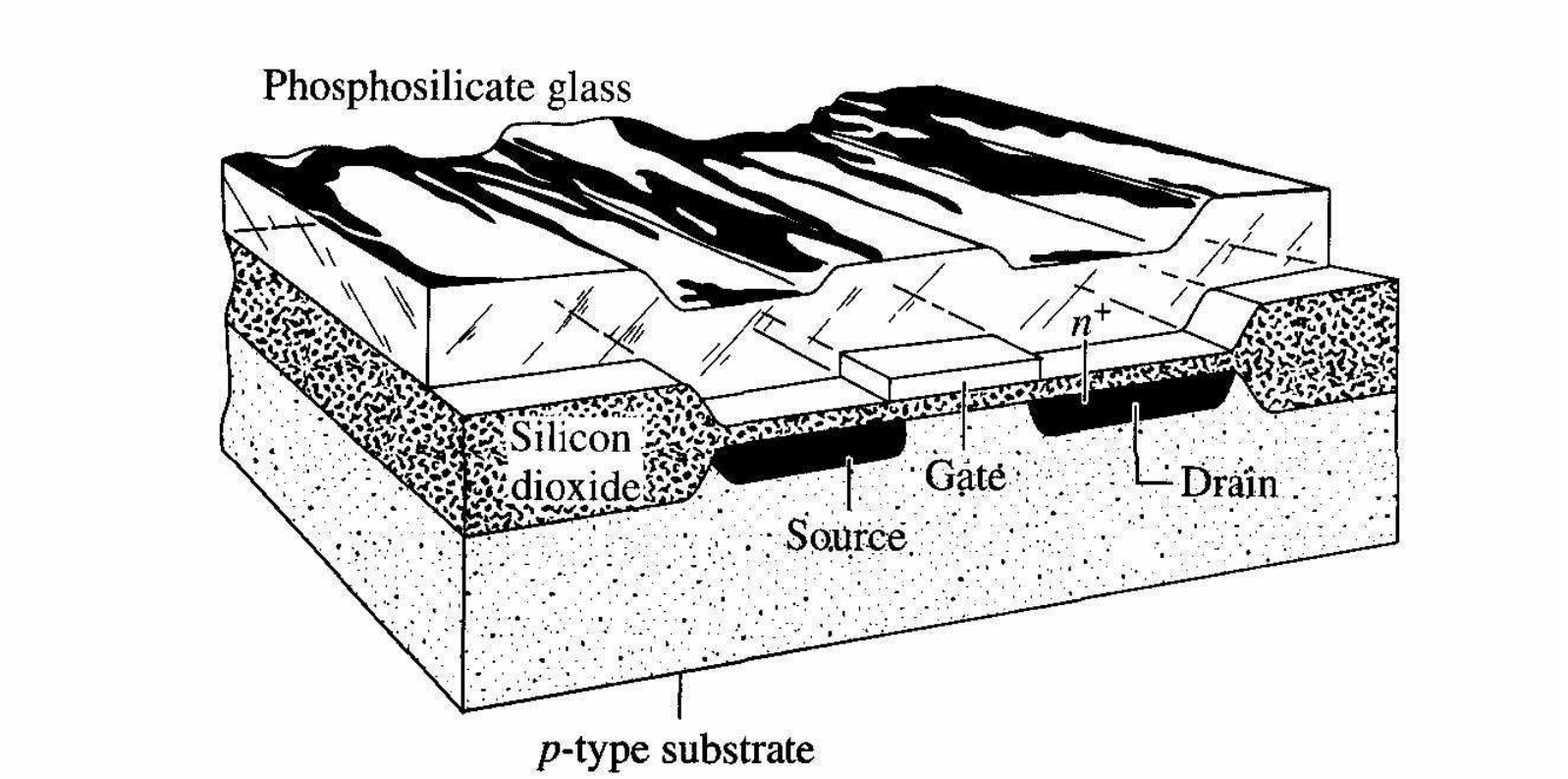


 Tunneling results after N. Saks, *et al.*, IEEE Trans. Nucl. Sci., **31**(1249) 1984.

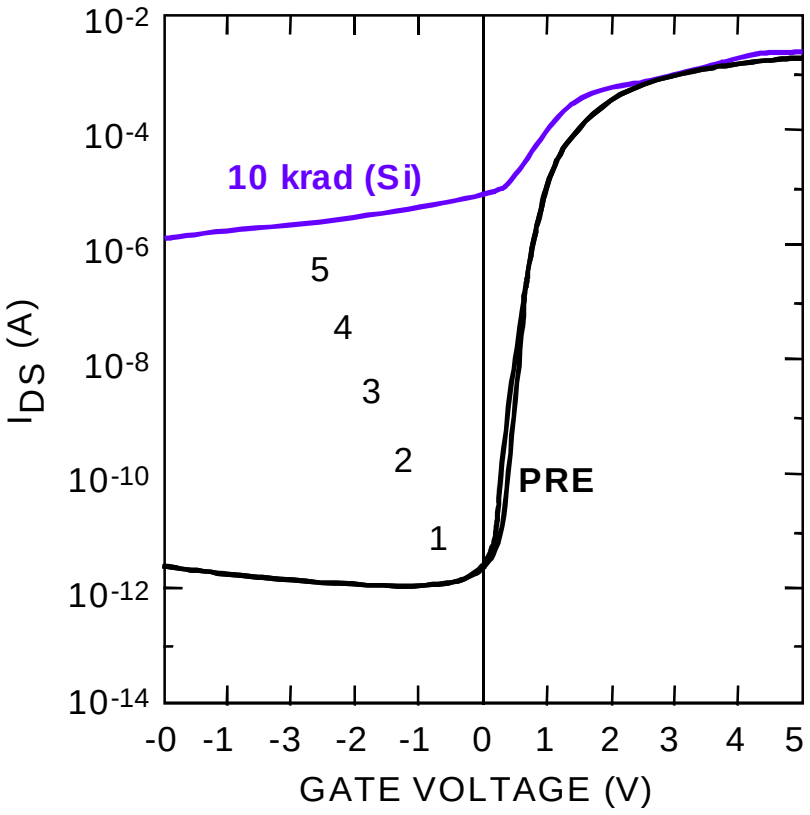
Cross Section of an MOS Transistor in an Integrated Circuit: Note the Isolation Regions

A silicon-dioxide region is used for lateral isolation in bulk CMOS

Total dose can increase leakage current in the isolation region



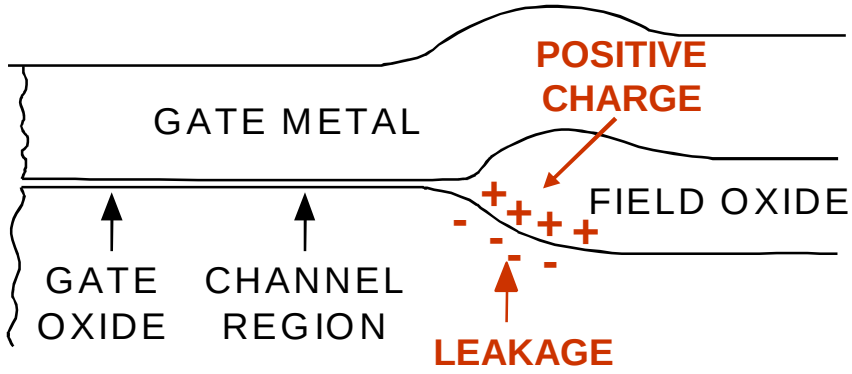
Field Oxide Leakage



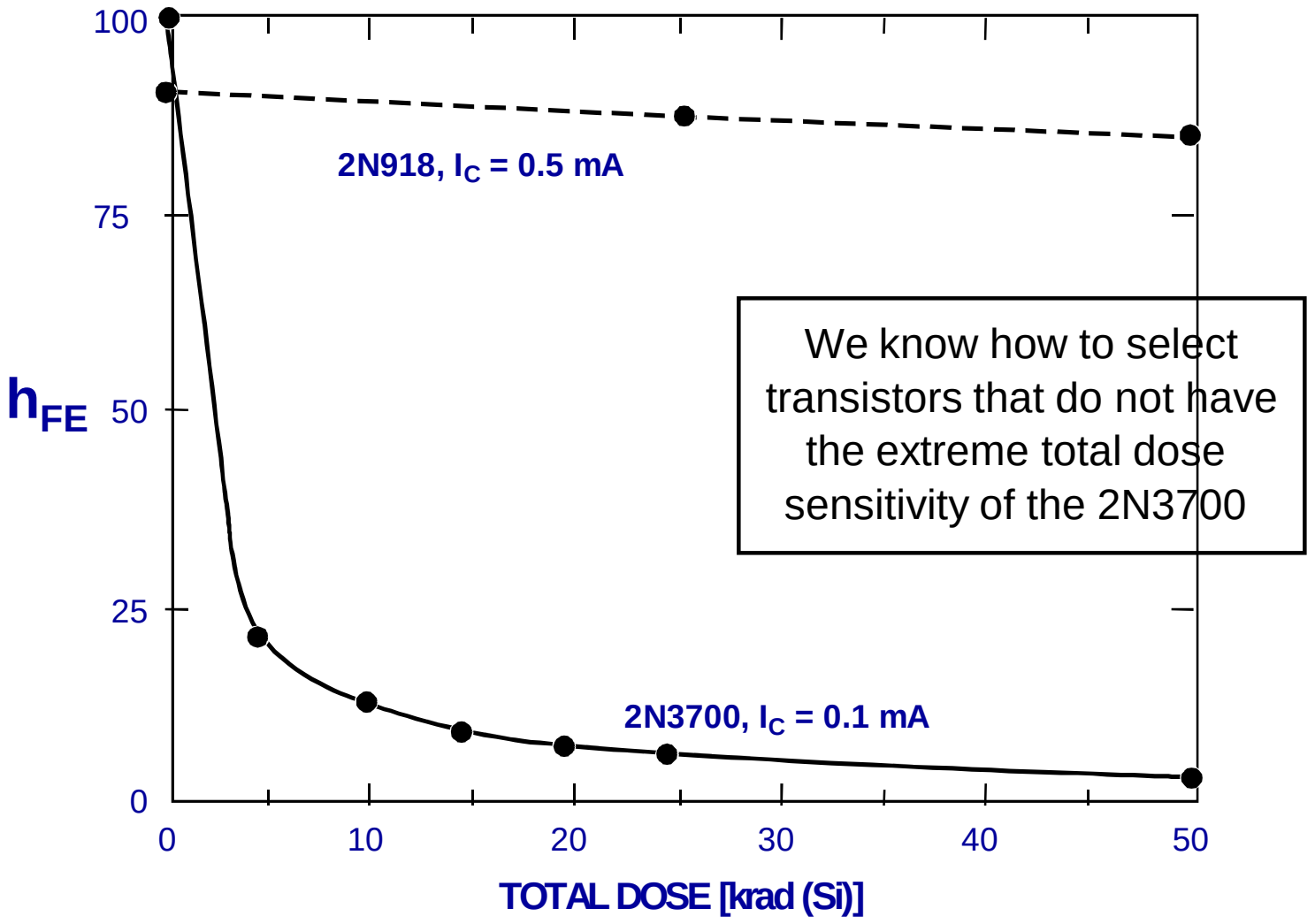
- Field oxides are much thicker than gate oxides

- Field-oxide leakage can be the dominant failure mechanism for commercial processes, causing a large change in leakage current

-The example shows charge trapping in a conventional field oxide



Total Dose Damage in Bipolar Transistor Used on the Cassini Spacecraft



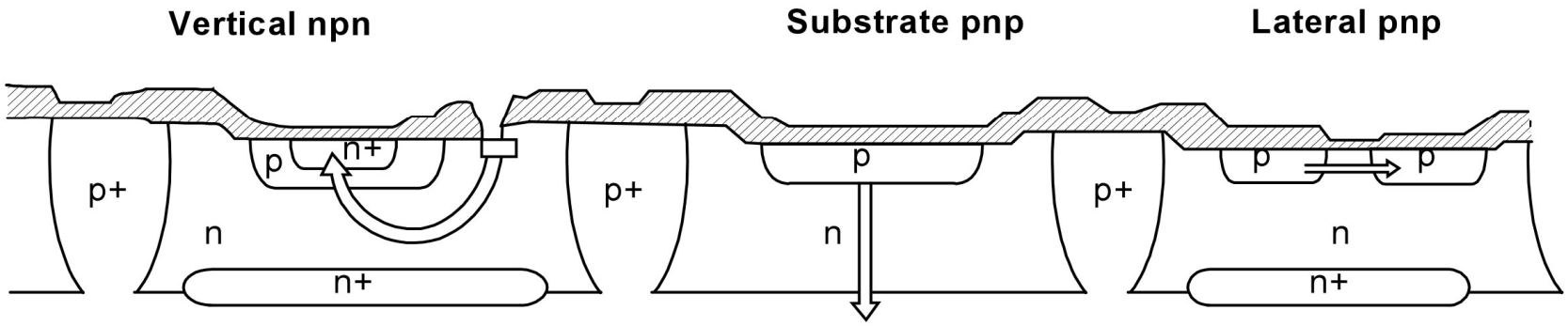
We know how to select transistors that do not have the extreme total dose sensitivity of the 2N3700

Internal Transistors in Bipolar Integrated Circuits

Basic process is rated for 36 V (legacy condition)

Optimized for npn transistors

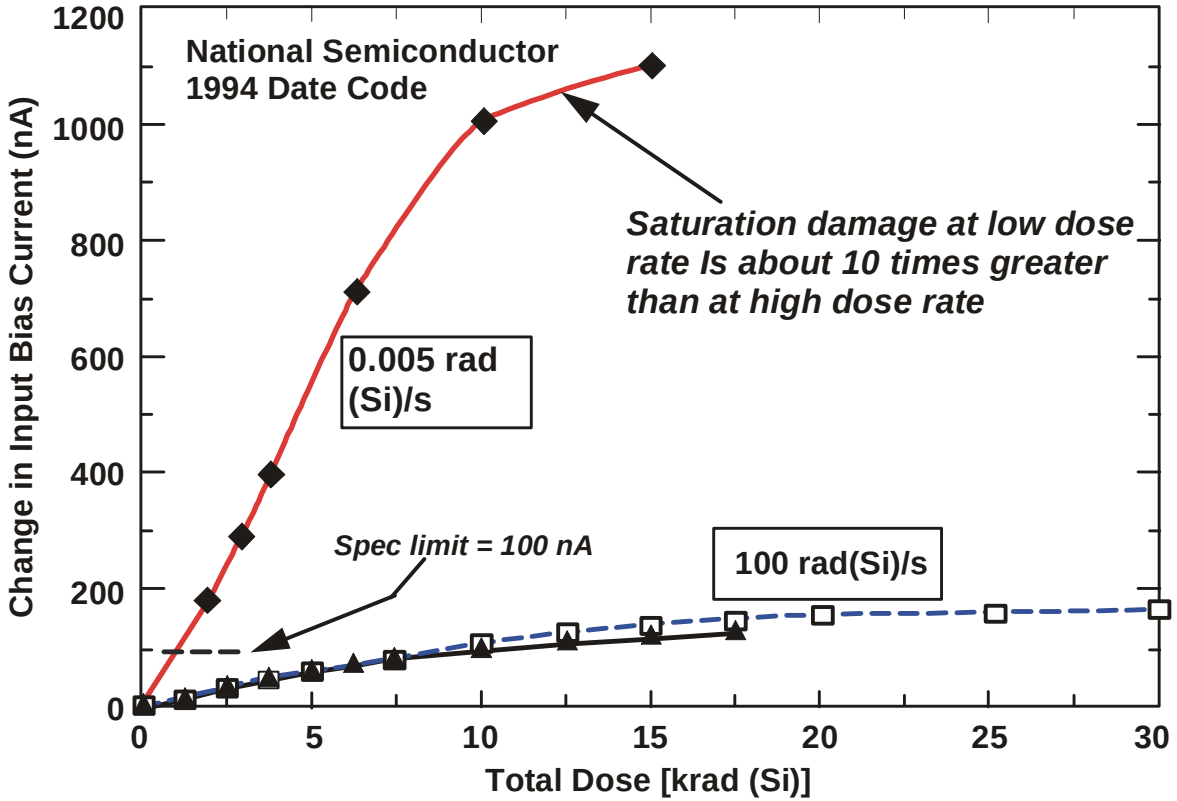
The two pnp transistors are “compromises” that do not require extra processing steps



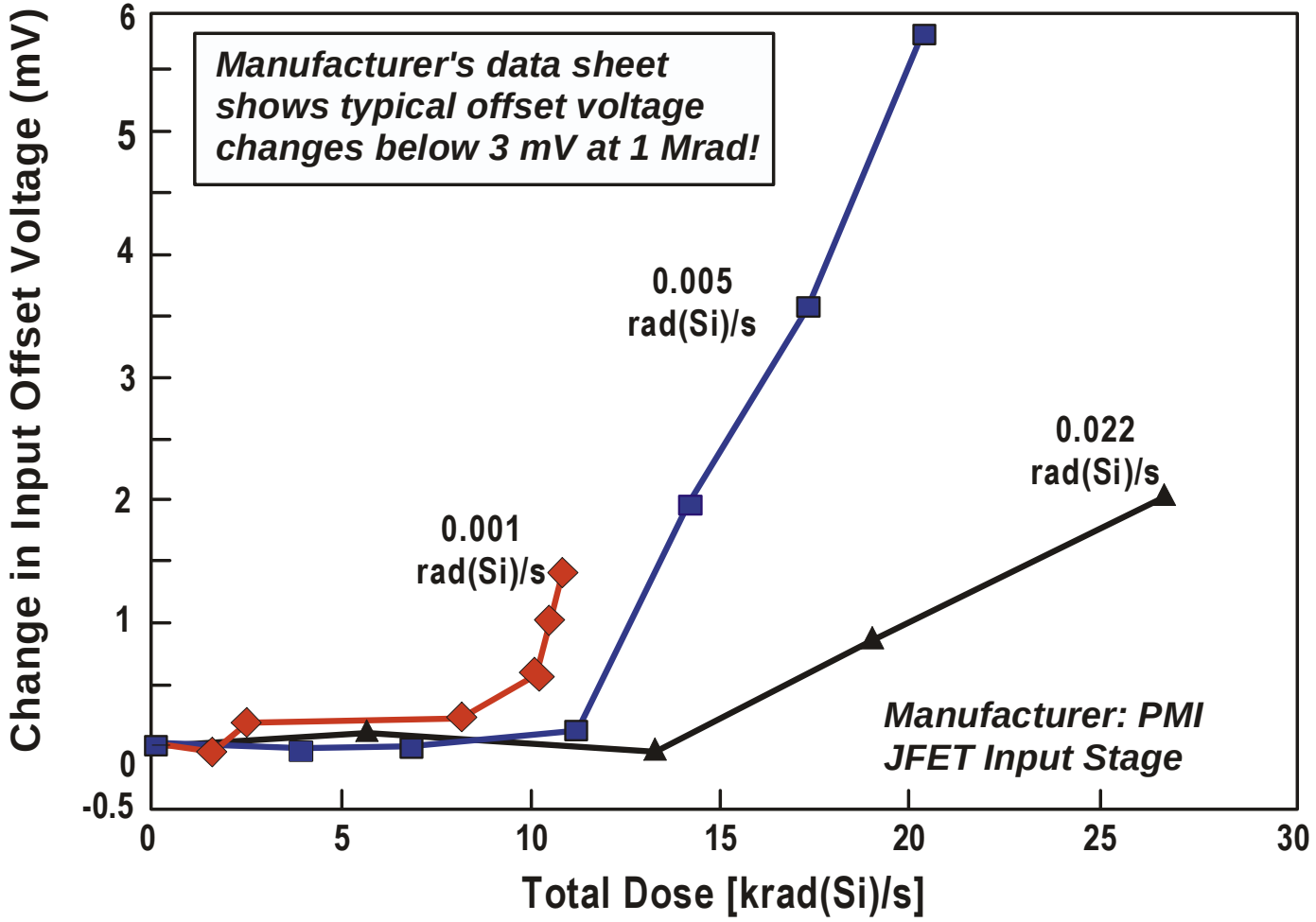
Enhanced Low Dose Rate Damage (ELDRS)

Damage in linear integrated circuits can be much more severe at low dose rates

The “compromise” pnp transistors are the most sensitive to this effect



A More Extreme Example: OP-42 Op-Amp



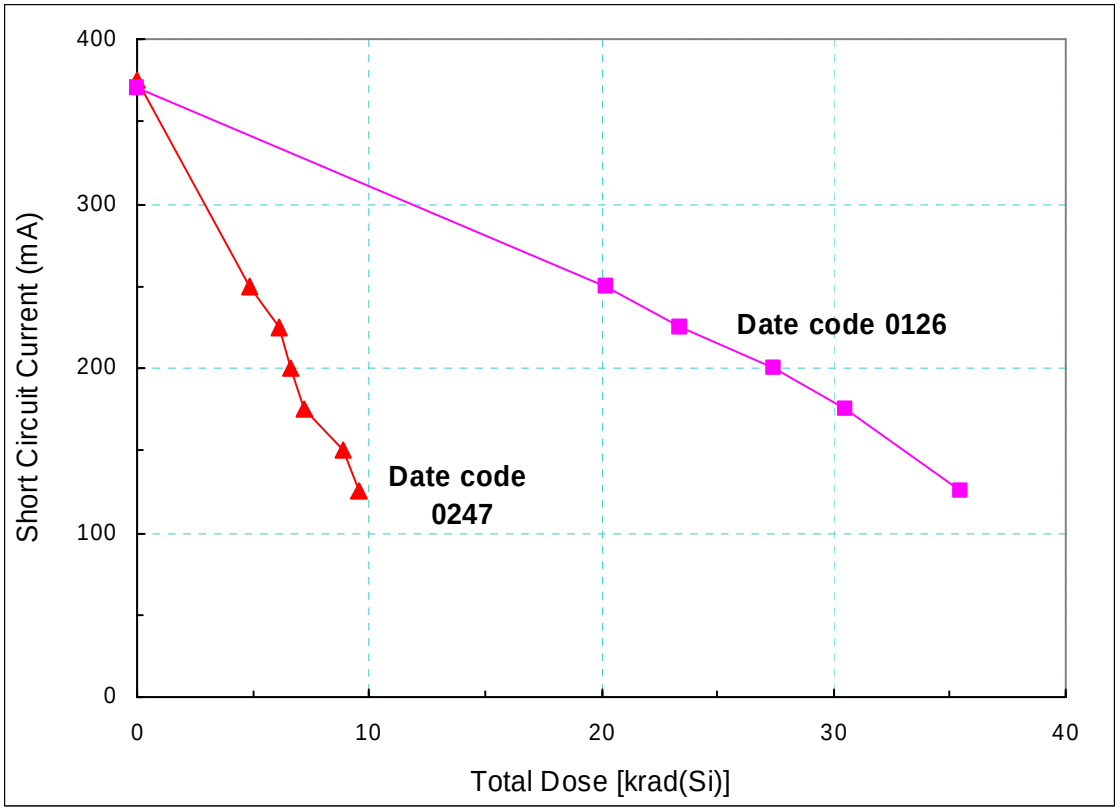
A. H. Johnston, *et al*., IEEE Trans. Nucl. Sci., **43**(3049), 1996.

Lot Variability of Total Dose Degradation of a Voltage Regulator

The output current is rated at 250 mA

Linear circuits designs can be very complex. Recent results have shown that certain types of voltage regulators are extremely sensitive to total dose damage.

The damage varies considerably between different production lots



T. F. Miyahira, *et al.*, 2005 Radiation Effects Data Workshop, p. 127.

Dealing with the Low Dose Rate Problem

- Bipolar Integrated Circuits ***Must*** Be Tested at Low Dose Rate
  - Time consuming, but necessary
  - Hardened parts are available from some manufacturers
  - Data base results are not reliable: testing problems and device variability affect results
- Some Bipolar ICs Do Not Exhibit ELDRS
  - High-performance vertical pnp transistors eliminate the need for thick isolation oxides
  - Some conventional linear processes are also immune to ELDRS

Example: Analog Devices

- Very little ELDRS effect for many of their devices
- However, extreme sensitivity for op-amps with JFET input stages

Warnings and Common Misperceptions

- "Off" circuit (no applied bias) does not mean that no damage will occur
  - Linear IC's can exhibit ***more*** damage when unbiased
  - Discrete transistor damage is about a factor of two lower when unbiased
  - CMOS bias effects are very complex
    - Generally some improvement when parts are unbiased
    - Needs to be checked on part-by-part basis

- Radiation data is not "generic"
  - Do not assume that data from one manufacturer applies to same part type from another manufacturer
  - Radiation response may change as manufacturing process evolves

- Characterization data must encompass use conditions
  - Example: linear IC data with +/- 15V power supplies cannot be used for 5/0 V applications
  - Total dose data bases are of limited value except for initial part selection
  - ELDRS must be accounted for in all bipolar and BiCMOS technologies

Total Dose Testing

Test Standards Were Originally Based on Military Environments

- High dose rate was mandated, and used for many years
- Low dose rate effects were not discovered until 1991, even though the same part technology had been in production for more than 20 years

Problem 1: Low Dose Rate

- Bipolar: test at low dose rate (10 mrad/s or less)
  - Straightforward, except that tests are time consuming
  - Many workers “cheat”, using higher dose rates
- CMOS: complex test methodology
  - Over-test to 1.5 times required level
  - Anneal at 125 C to allow trapped hole annealing, and test devices
  - Problem: only provides data at a single total dose level

Problem 2: Gamma Rays Are Inappropriate for Space

- This leads to the next topic, displacement damage

Dealing with the Total Dose Problem

Testing and qualifying devices at these radiation levels is difficult and expensive

- "Archival" data is indicative only
- Tests on specific lots used on the mission are required

Shielding is a difficult option because of the mass penalty

The mission is planning on three different levels

- 1 Mrad (100 mil shield)
- 300 krad (additional shielding)
- 100 krad (limited to as few cases as possible)

The APML is the preferred solution to the high total dose problem

The Europa project takes care of the costly issues of testing and qualification of parts on the APML

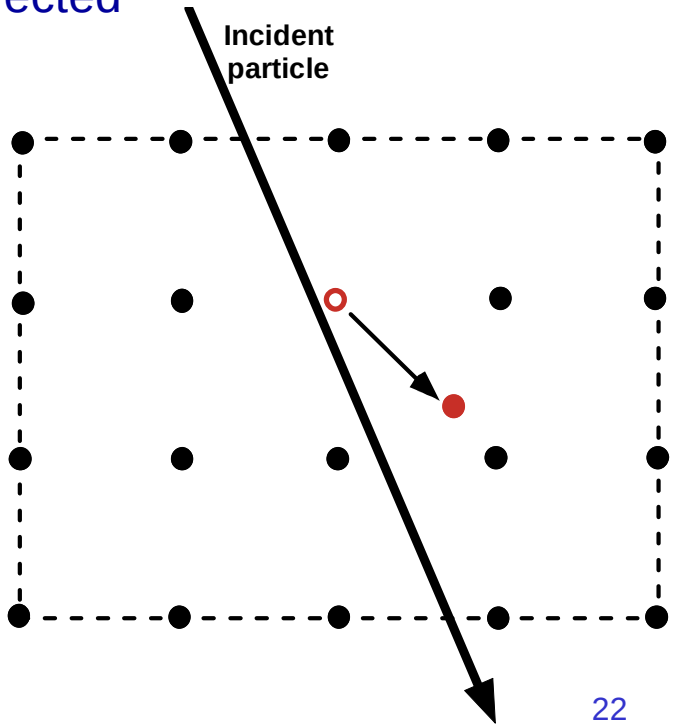
Displacement Damage

Effects of Displacement Damage in Semiconductors

- Minority carrier lifetime is degraded
  - Reduces gain of bipolar transistors
  - Also affects optical detectors and some types of light-emitting diodes
  - Effects become important for proton fluences above 10^{10} p/cm^2
- Mobility and carrier concentration are also affected
  - Only important for high fluences

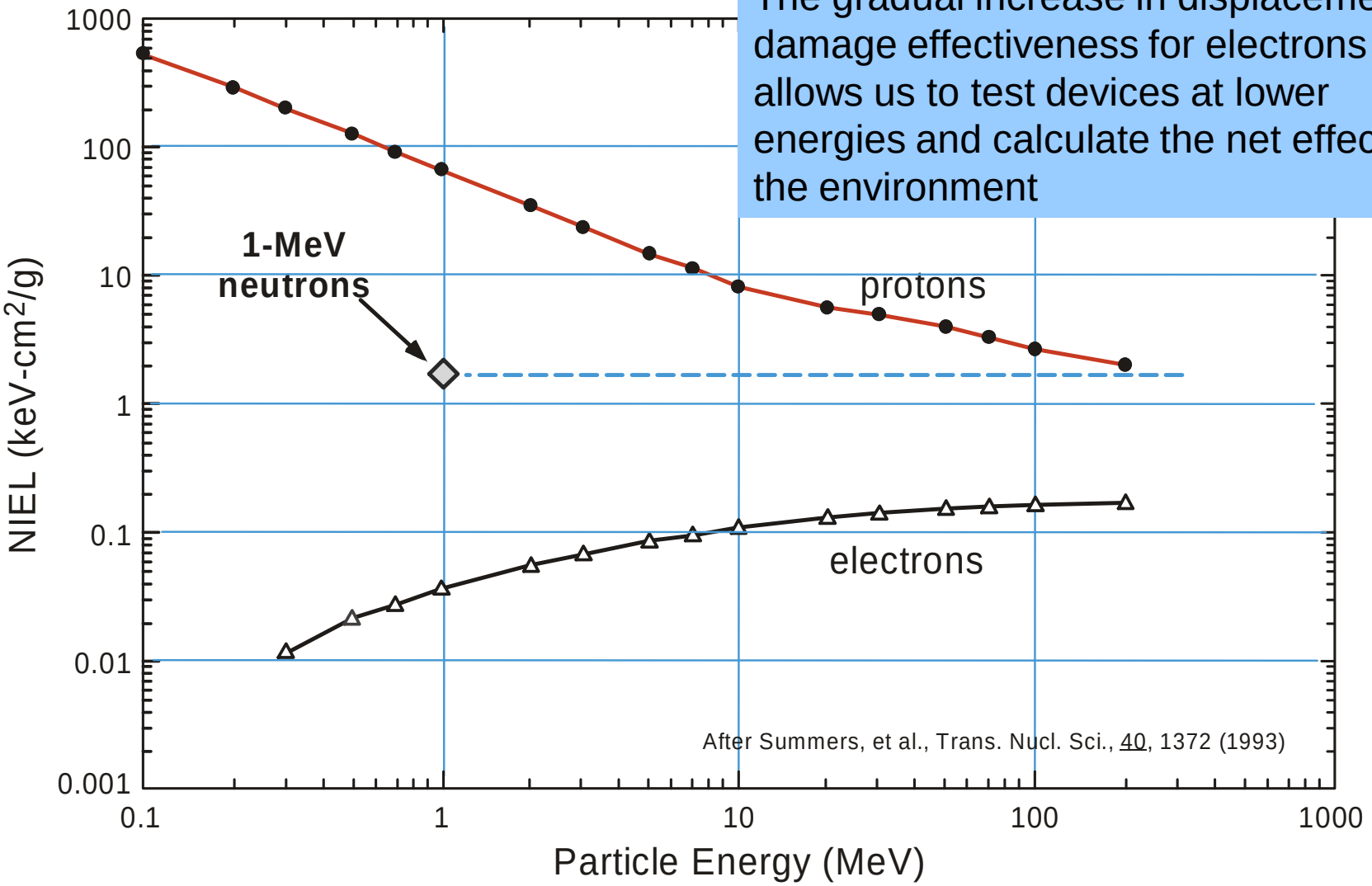
Particles Producing Displacement Damage

- Protons (all energies)
- Electrons with energies above 150 keV
- Neutrons (from on-board power sources)



Energy Dependence of Displacement Damage in Silicon

The gradual increase in displacement damage effectiveness for electrons allows us to test devices at lower energies and calculate the net effect in the environment



Dealing with the Energy Dependence

Usually displacement damage tests are done at only a single energy

- Too costly to use multiple energies
- Proton test data can generally be used in lieu of electron data

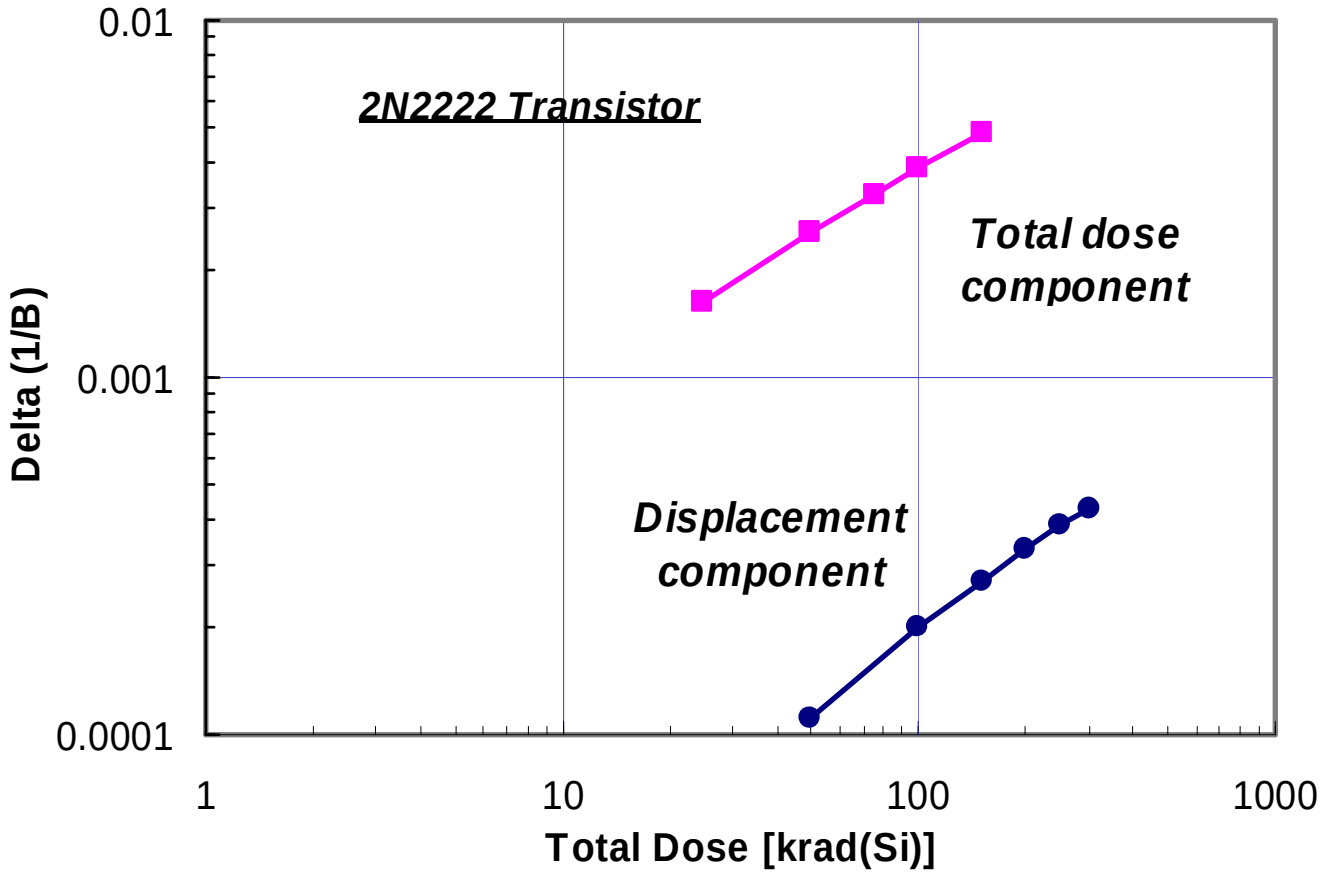
The effect of the damage is determined by weighting the damage in each energy interval, and integrating the weighted values over the energy spectrum

Non-ionizing energy loss (NIEL) is used to normalize damage from different energies and particle types

- Useful concept, but not always accurate
- NIEL describes displacement energy process, not the *net* damage in devices
- Annealing is very important, and can affect the results

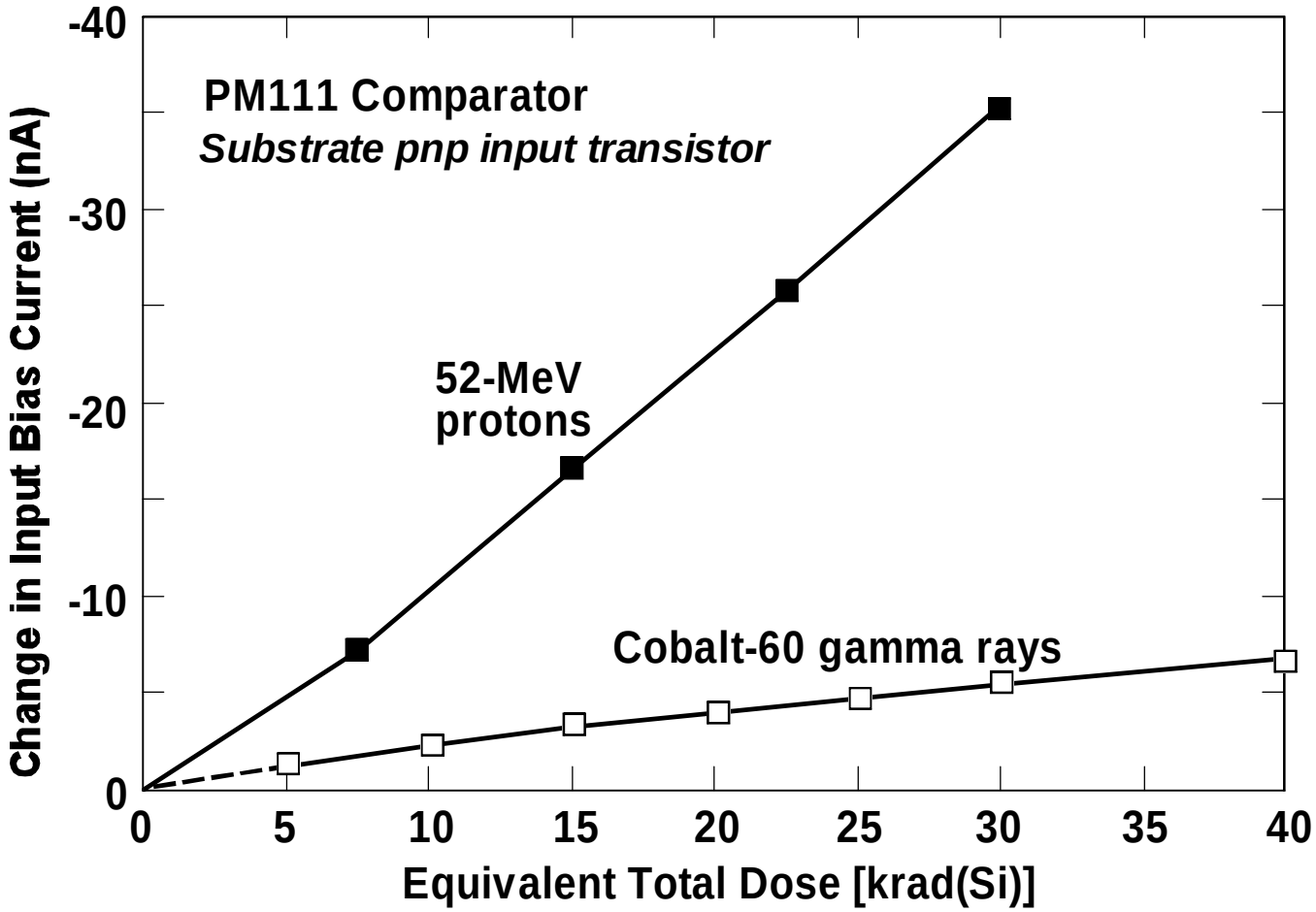
Total Dose and Displacement Damage for 2N2222 Transistor

Displacement damage can usually be ignored for conventional transistors with narrow base widths



Effects of Gamma and Proton Irradiation on Input Bias Current of a Differential Comparator

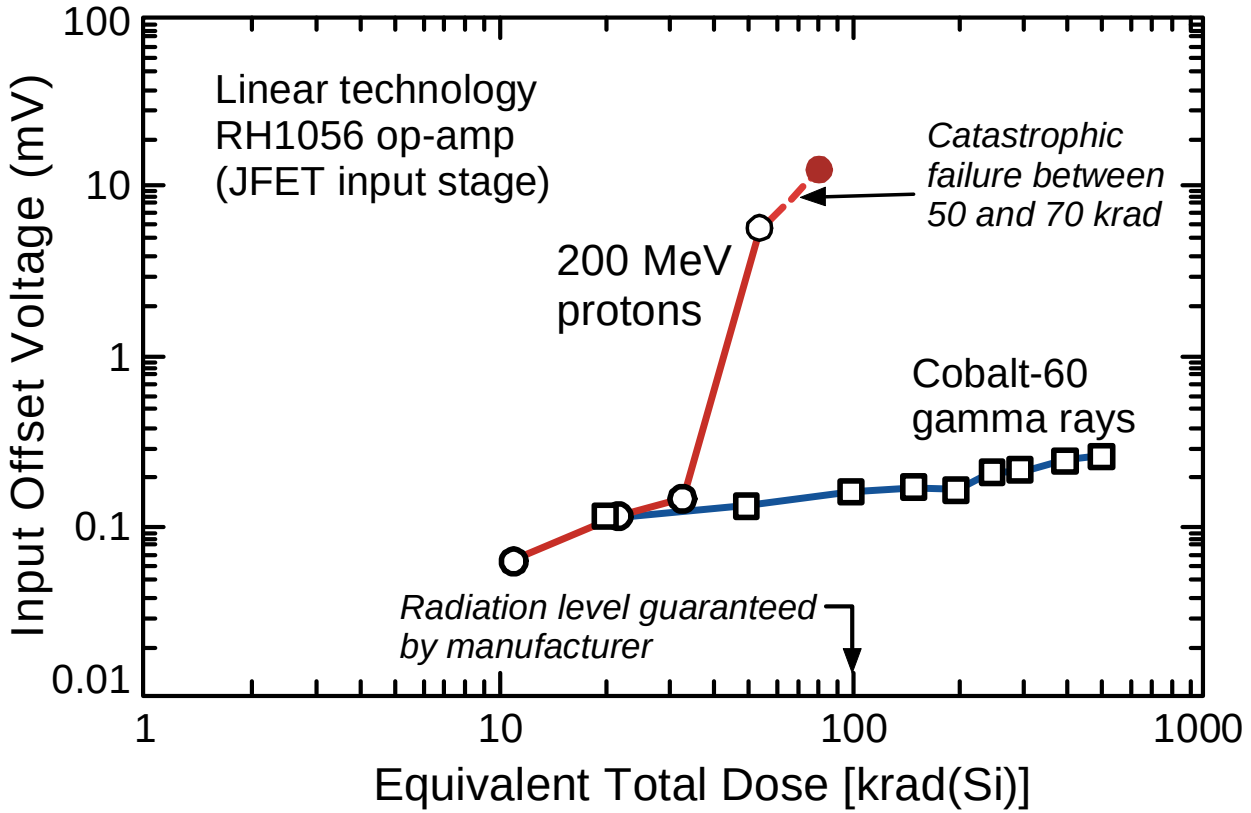
The wide base pnp transistors in linear ICs are very sensitive to displacement damage



B. G. Rax, *et al.*, IEEE Trans. Nucl. Sci., **45**(2632 (1998).

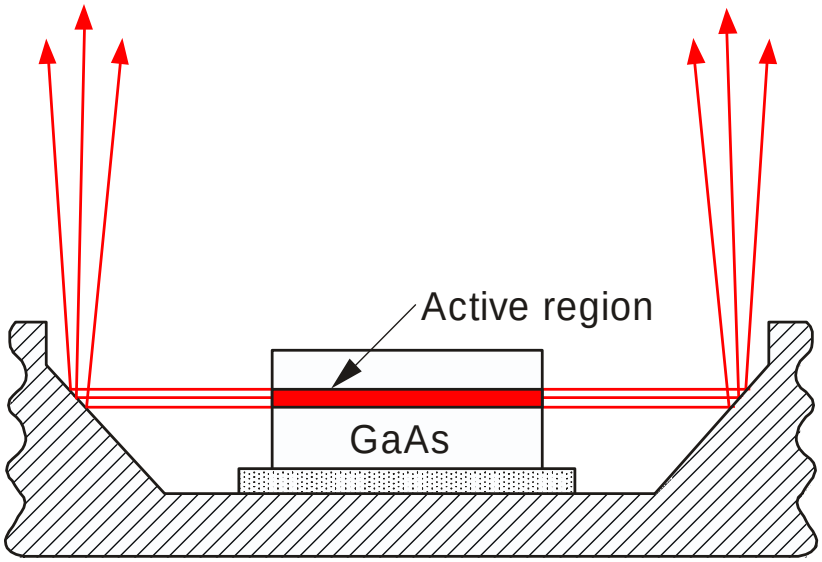
Displacement Damage in a Hardened Op-Amp

This shows that their can be a large difference between total dose lab test results and the damage that will occur in the real space environment.

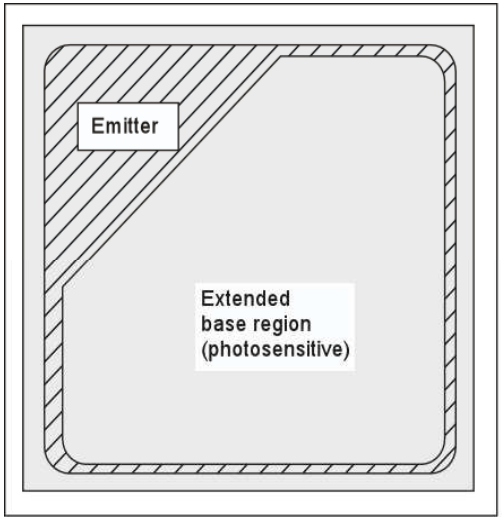


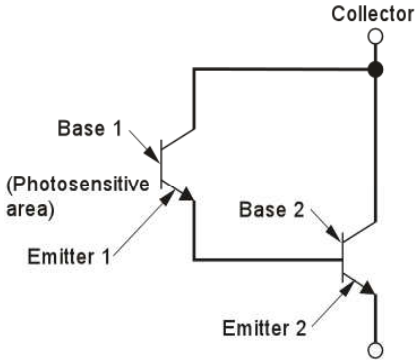
B. G. Rax, *et al.*, IEEE Trans. Nucl. Sci., **45**(2632 (1998).

Displacement Damage in Optoelectronic Devices



We will use 50 MeV protons as a reference point for discussing displacement damage in photonic devices





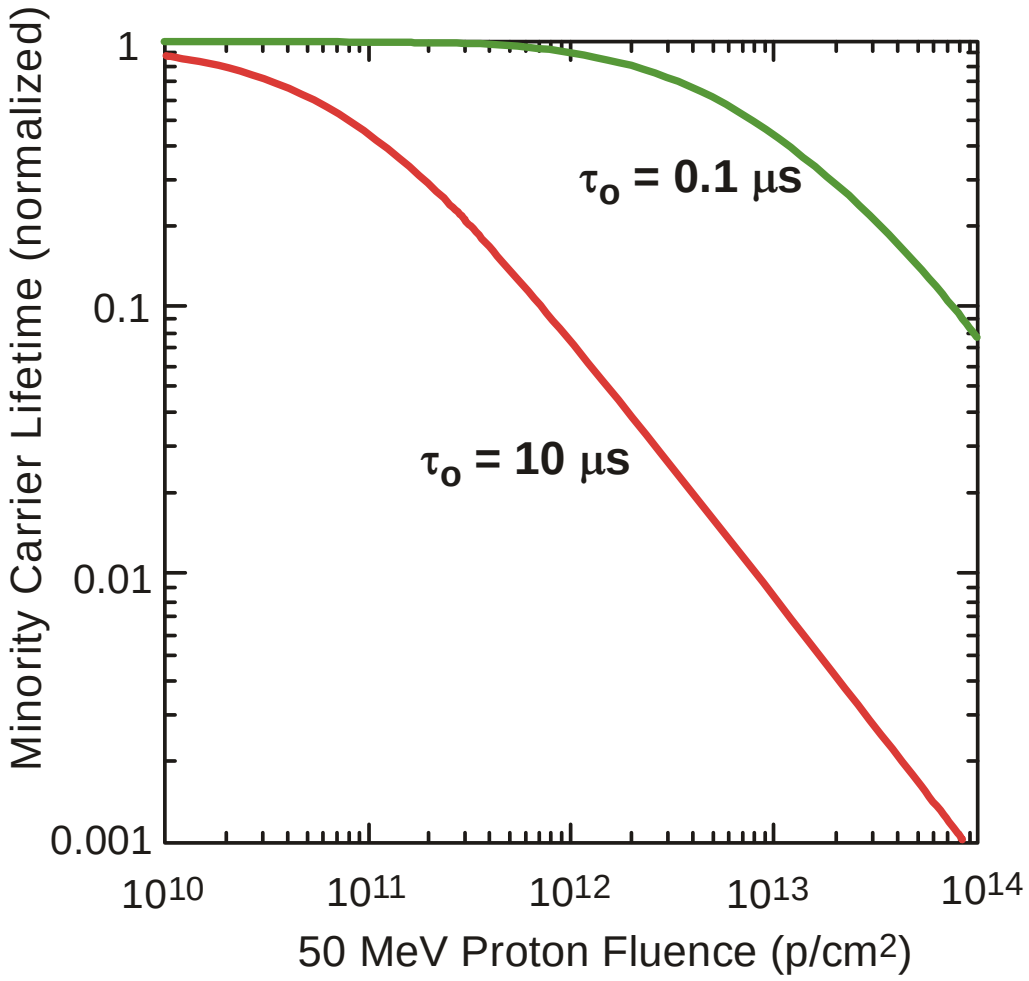
Carrier Transport Lengths

Recombination centers reduce minority carrier lifetime and diffusion length

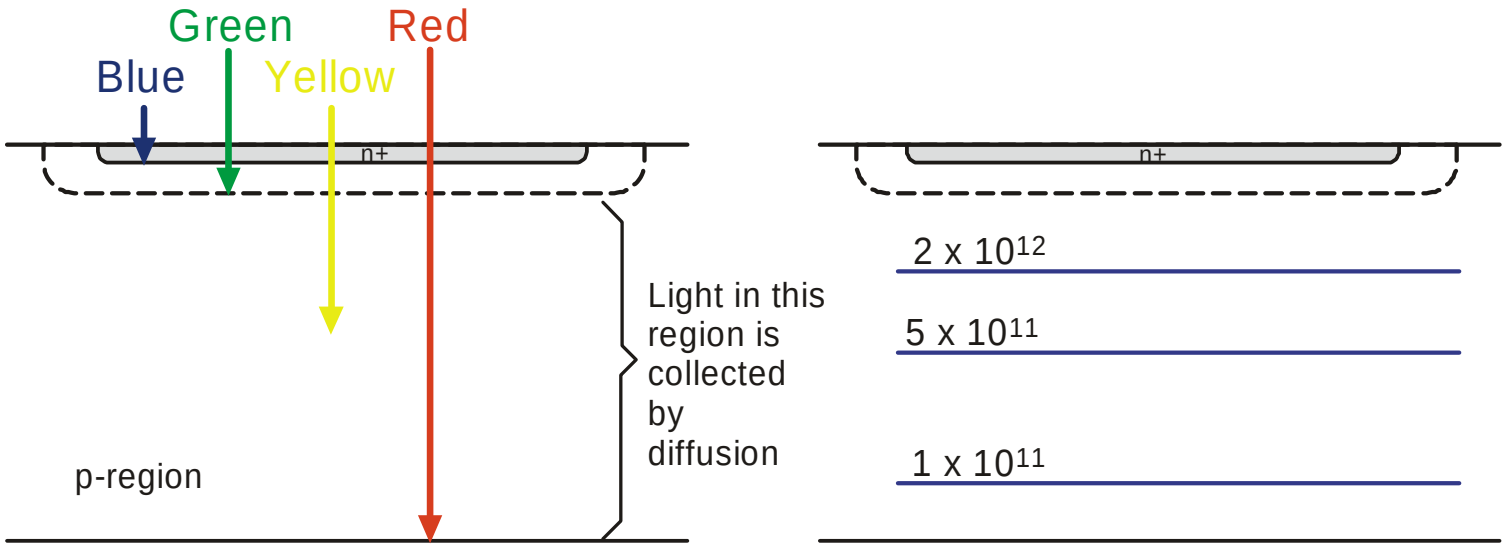
Described by

$$\frac{1}{\tau} - \frac{1}{\tau_o} = \frac{\Phi}{K}$$

Carrier Diffusion Lengths	
2N2222 transistor	0.6 μm
substrate pnp transistor	3 μm
silicon phototransistor	50 μm
880 nm LED	100 μm



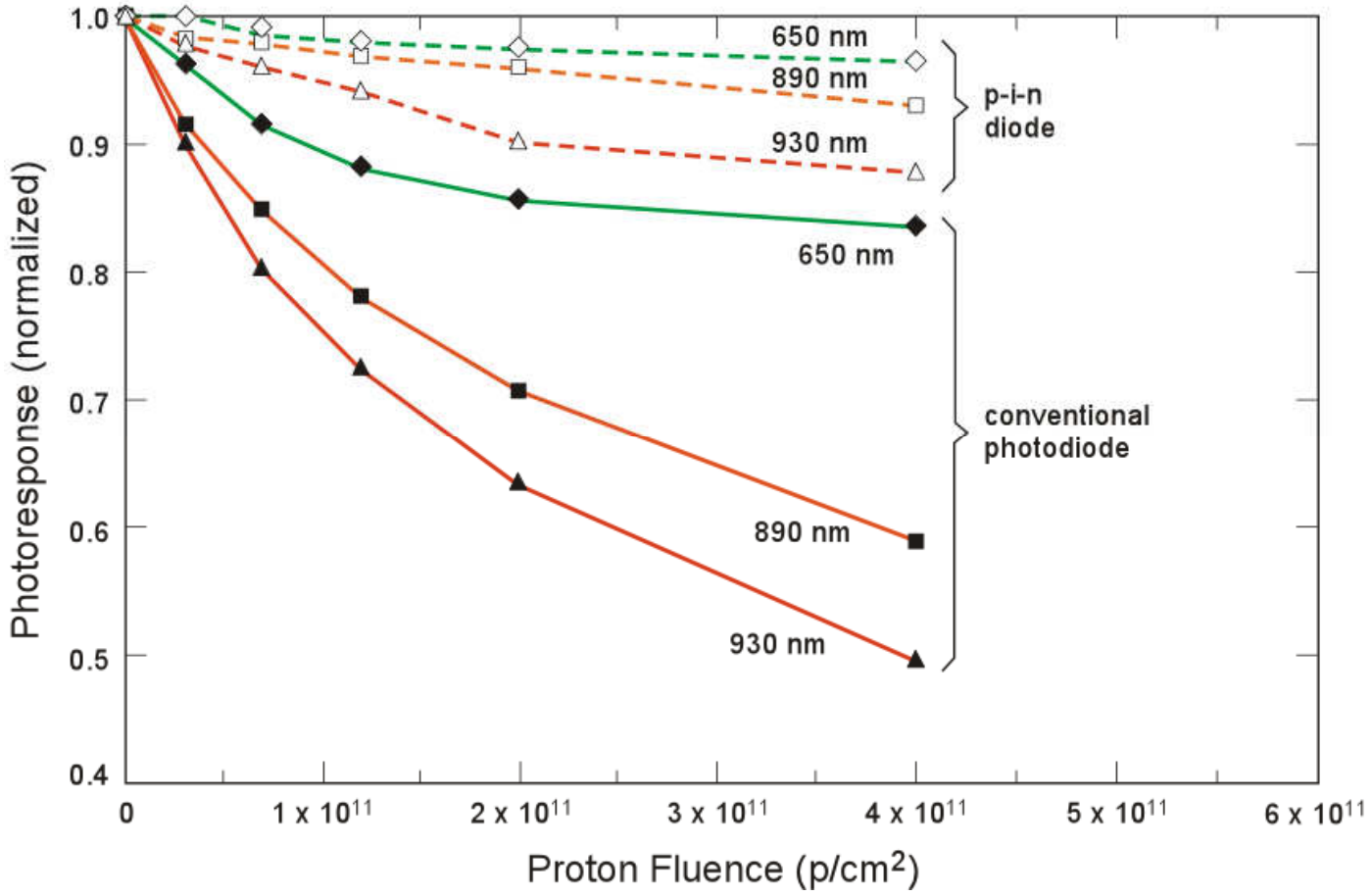
Light Absorption in a Basic Silicon p-n Photodiode



(a) Absorption by Various Wavelengths

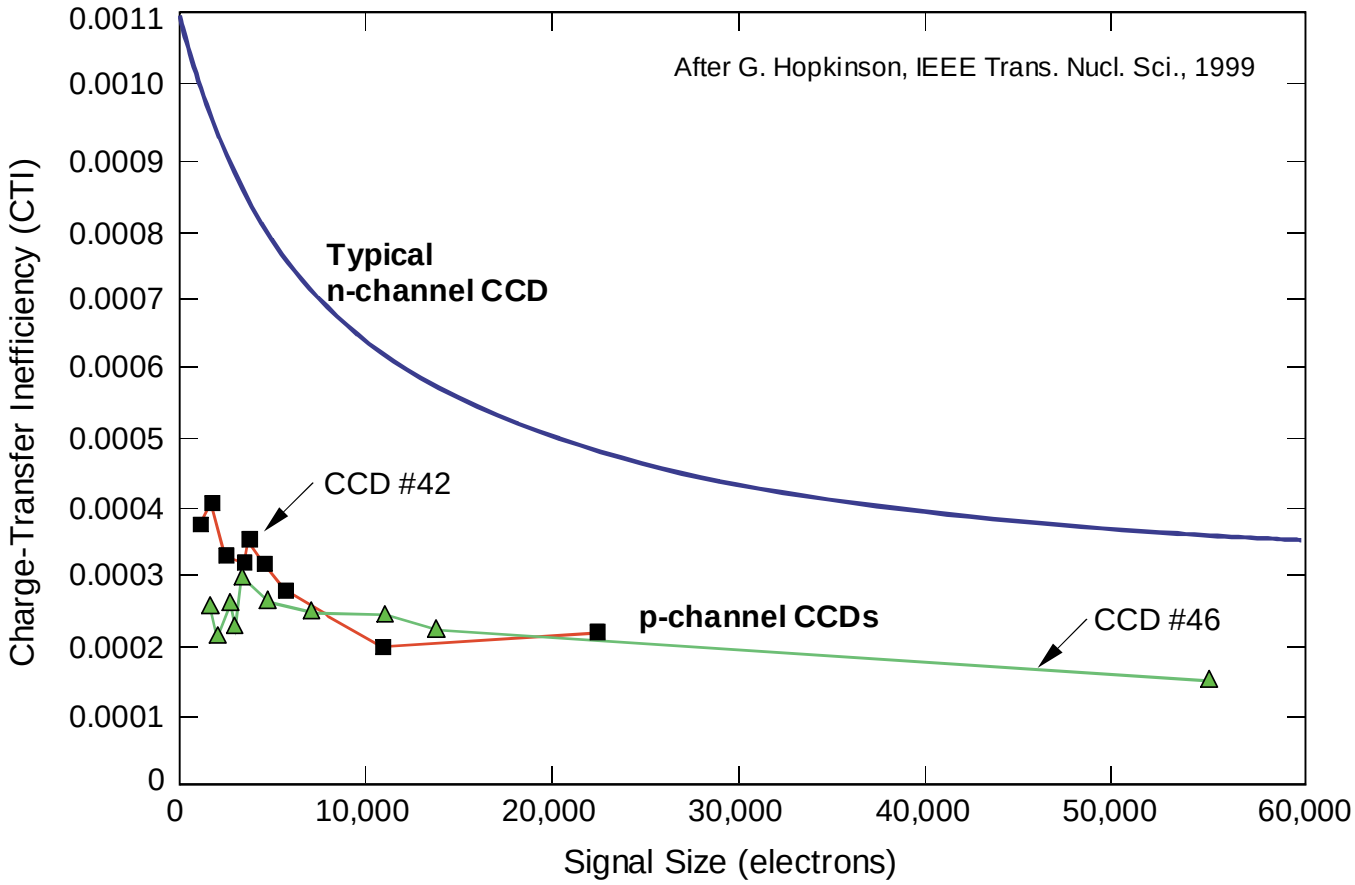
(b) Diffusion Length After Irradiation with 50-MeV Protons: $L = \sqrt{D\tau}$

Degradation of Silicon Detectors



Charge Coupled Detectors

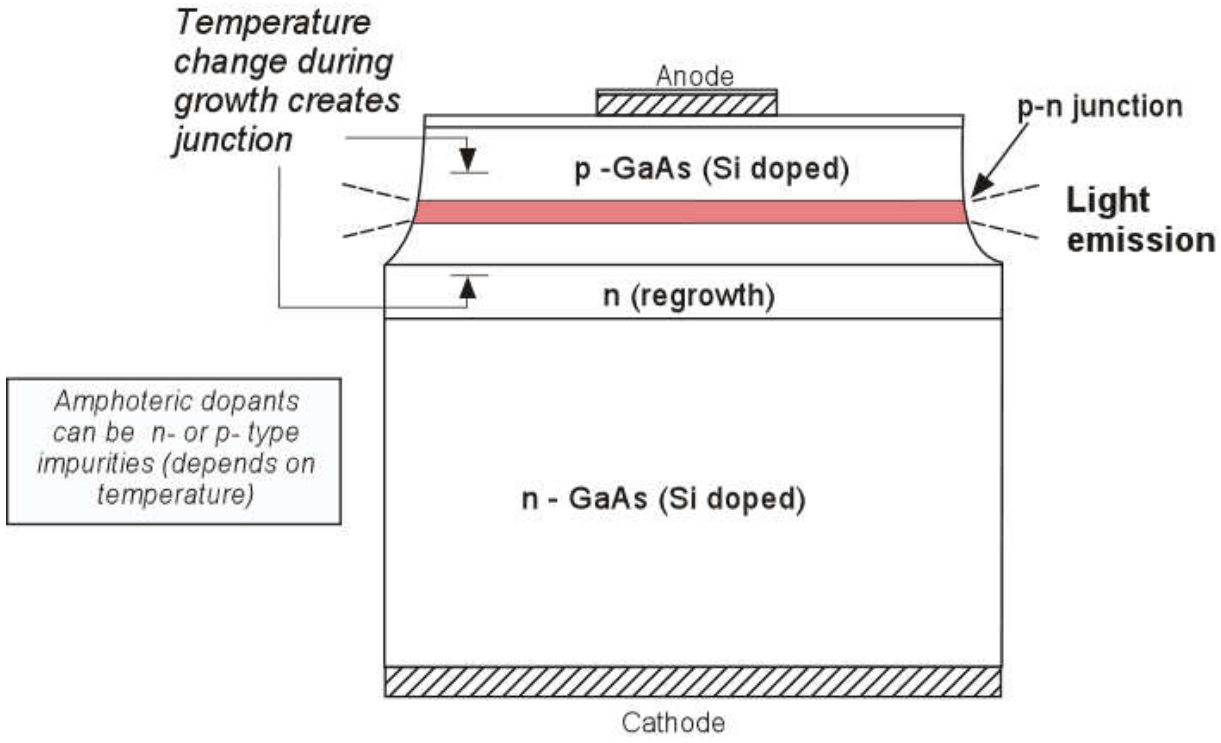
These results show how a fluence of 10^{10} p/cm^2 affects charge coupled detectors



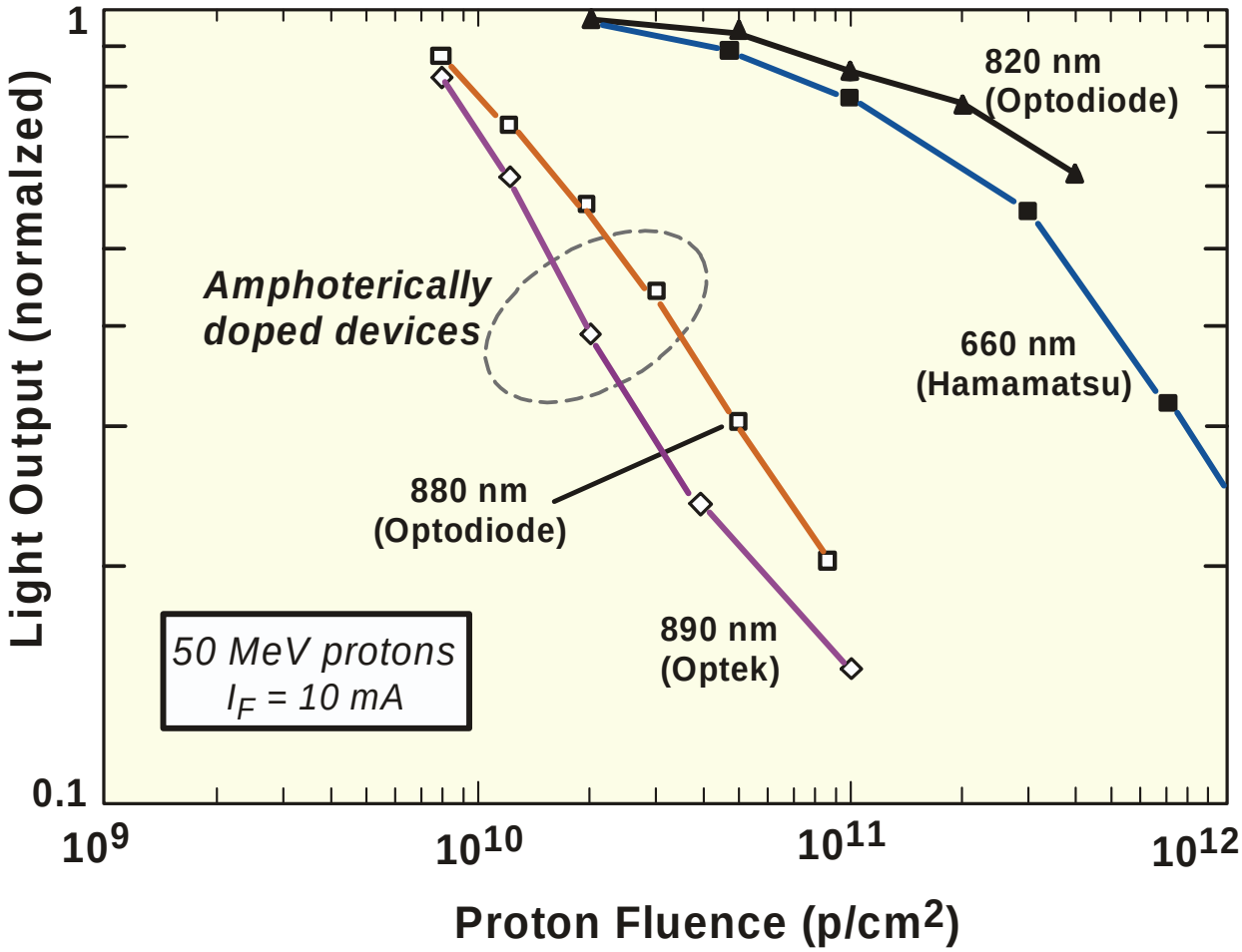
Displacement Damage in Light Emitting Diodes: Amphoterically Doped LEDs

Highly doped device, causing offset between absorption and emission spectra within the LED (good efficiency)

Growth process results in very wide active region (~ 50 microns)



Degradation of Light-Emitting Diodes



A. H. Johnston, IEEE Trans. Nucl. Sci., **50**(689), 2003.

Summary of Optoelectronic Issues

Permanent damage in light emitting diodes is an important problem

- Ended Topex-Poseidon mission
- Also affected Galileo tape recorder (Jupiter) during last orbit
- Avoid amphoterically doped LEDs

Detector degradation can also be important

Optical fibers are relatively resistant to damage unless long fiber lengths are involved, or very low temperature

- Damage mechanism is formation of color centers, not displacement damage

Outline (continued): SEE Effects

Space Radiation Environment II: *Single-particle effects*

Single-Event Upset Mechanisms

SEU in CMOS

- Basic SEU effects
- SEU Effects in complex circuits
- Effects of device scaling

Catastrophic SEU Effects

- Latchup
- SEGR and SEB

Unlike total dose, the SEE problem for Europa is not very different from other mission in deep space

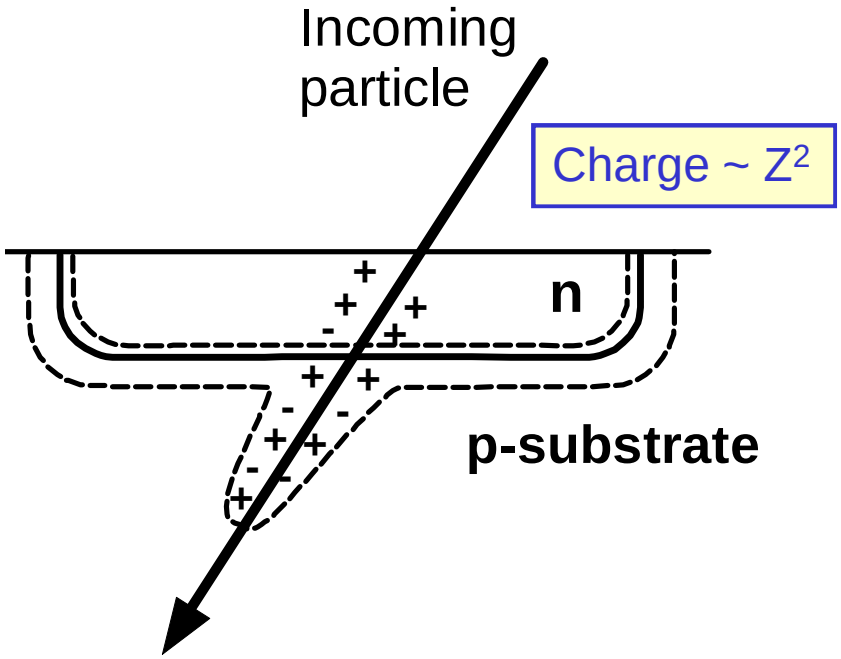
Galactic Cosmic Rays

Extremely energetic particles

- Produced by inter-galactic acceleration
- They occur everywhere in space

GCR particles produce an intense track of electron-hole pairs along their path

Charge collected in p-n junctions can cause a basic storage cell to change state (SEU)



Note the longer path length for strikes at angle

Other Properties

Standard Units:

MeV-cm^2/mg

In silicon, 1 MeV-cm^2/mg ~ 0.01 pC/μm

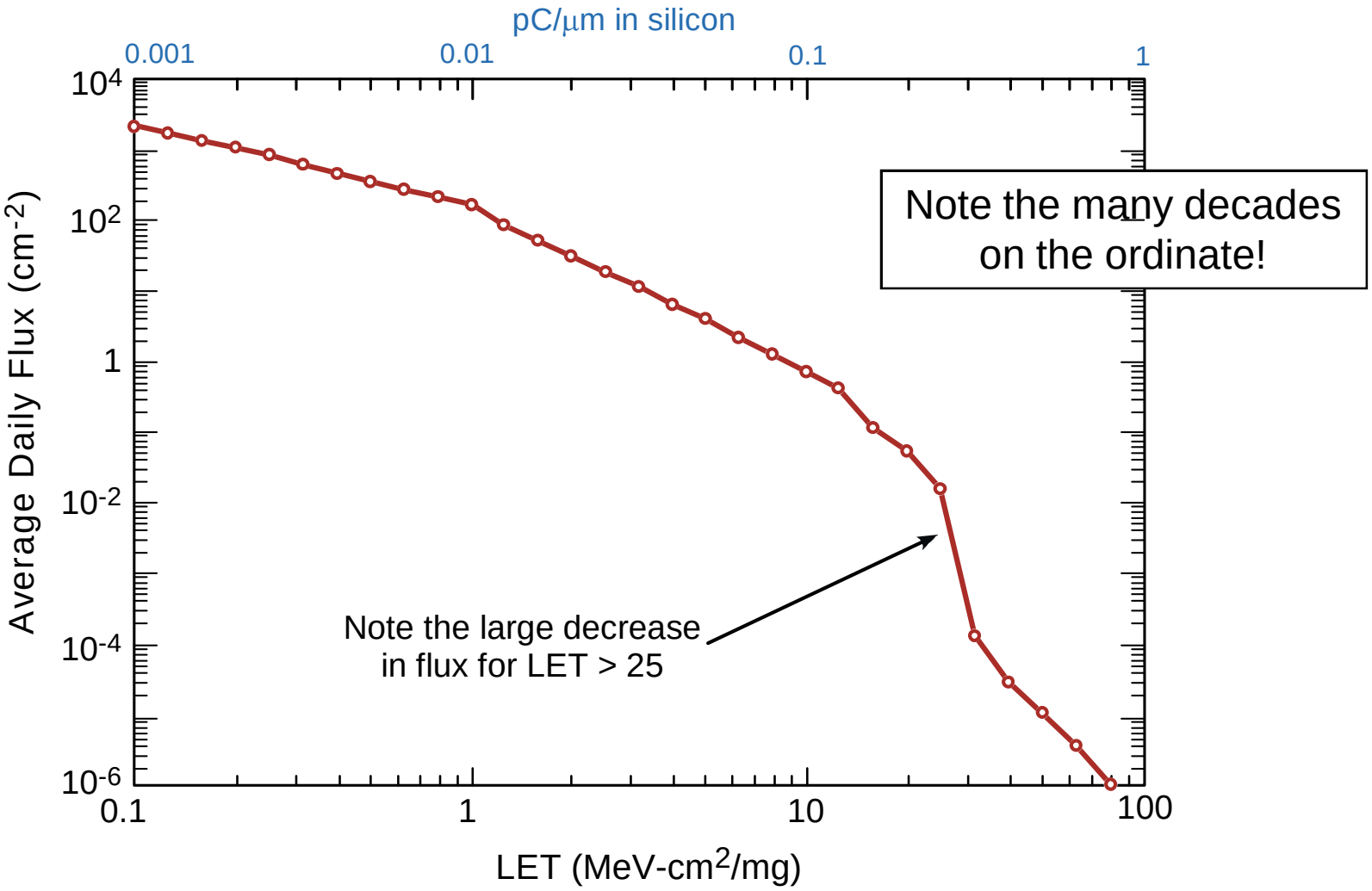
Slight modulation by solar activity

– (4X higher during solar ***minimum***)

Strikes at angle produce more charge

~ 1/cos (Θ)

Integral Cosmic Ray Spectra in Deep Space



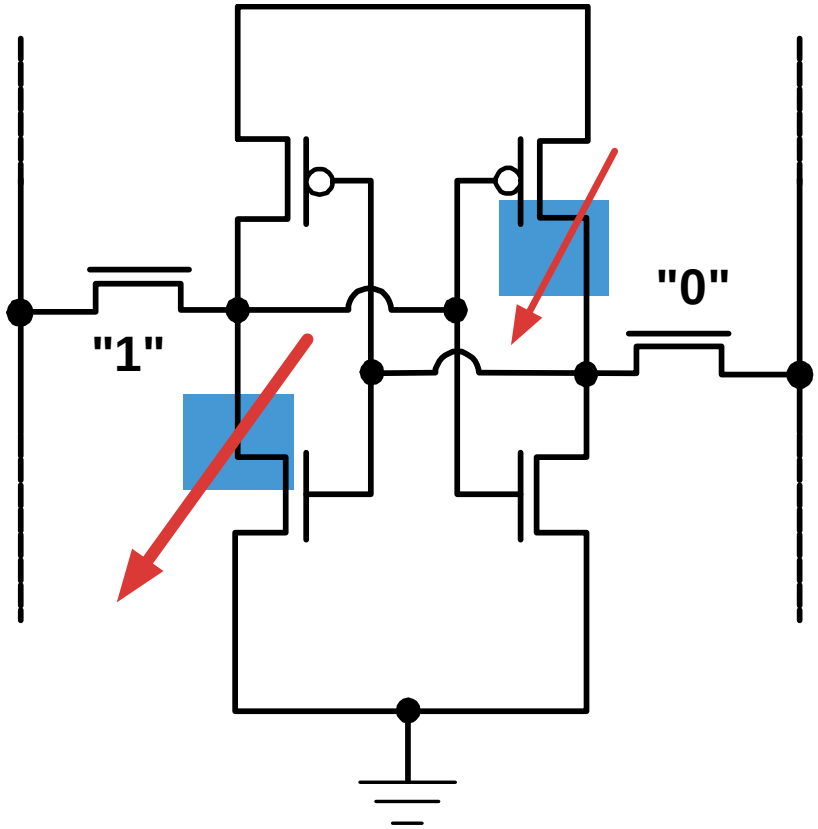
J. H. Adams, Jr., IEEE Trans. Nucl. Sci., **29** (2095), 1982.

Upset in an SRAM Cell

Upset occurs if the collected charge is above the critical charge for the circuit (Q_c)

Charge collected in drain region causes “off” device to turn on

“Off” NMOS device is the most sensitive node

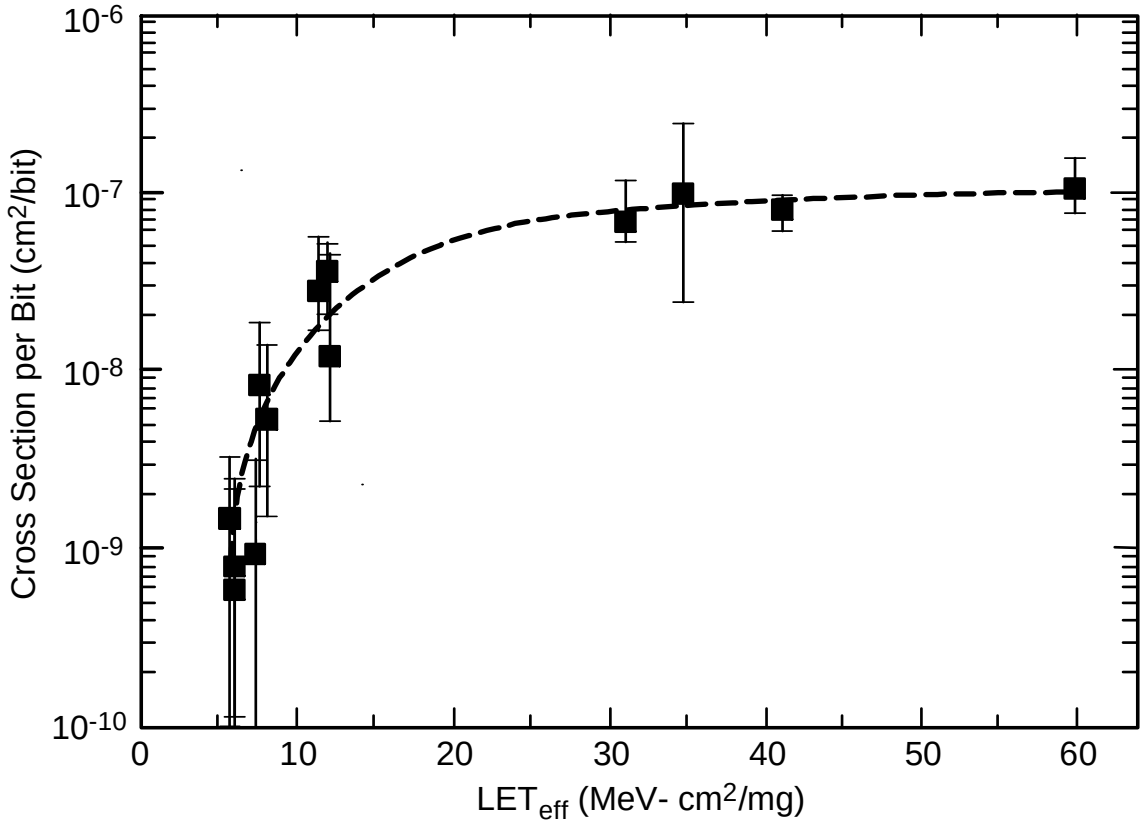


Experimental Cross Section Curve for Registers in a Microprocessor

Each data point corresponds to a different ion beam

The key parameters are the threshold LET and saturation cross section

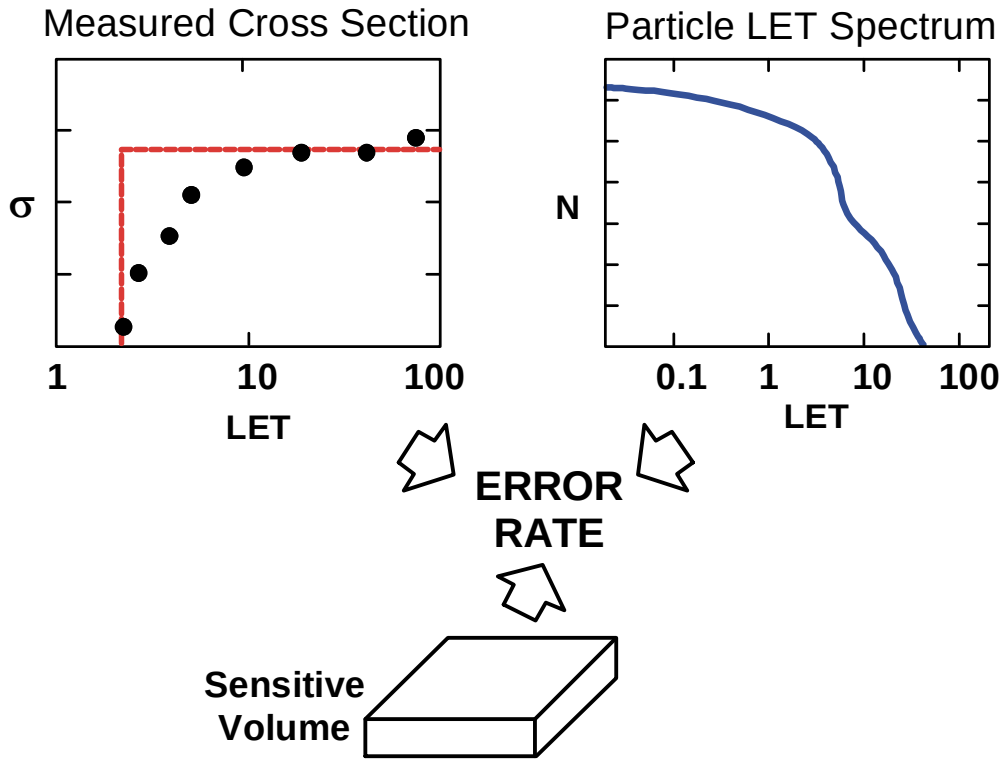
Error bars correspond to statistical counting uncertainty



Rate Calculations

Charge depends on sensitive volume
- Particles strike in any direction
- Volume shape determines effect of high-angle strikes

Rate depends on convolution of cross section and particle LET spectrum, along with the geometric effects of the charge collection geometry



Computer programs are available to perform rate calculations

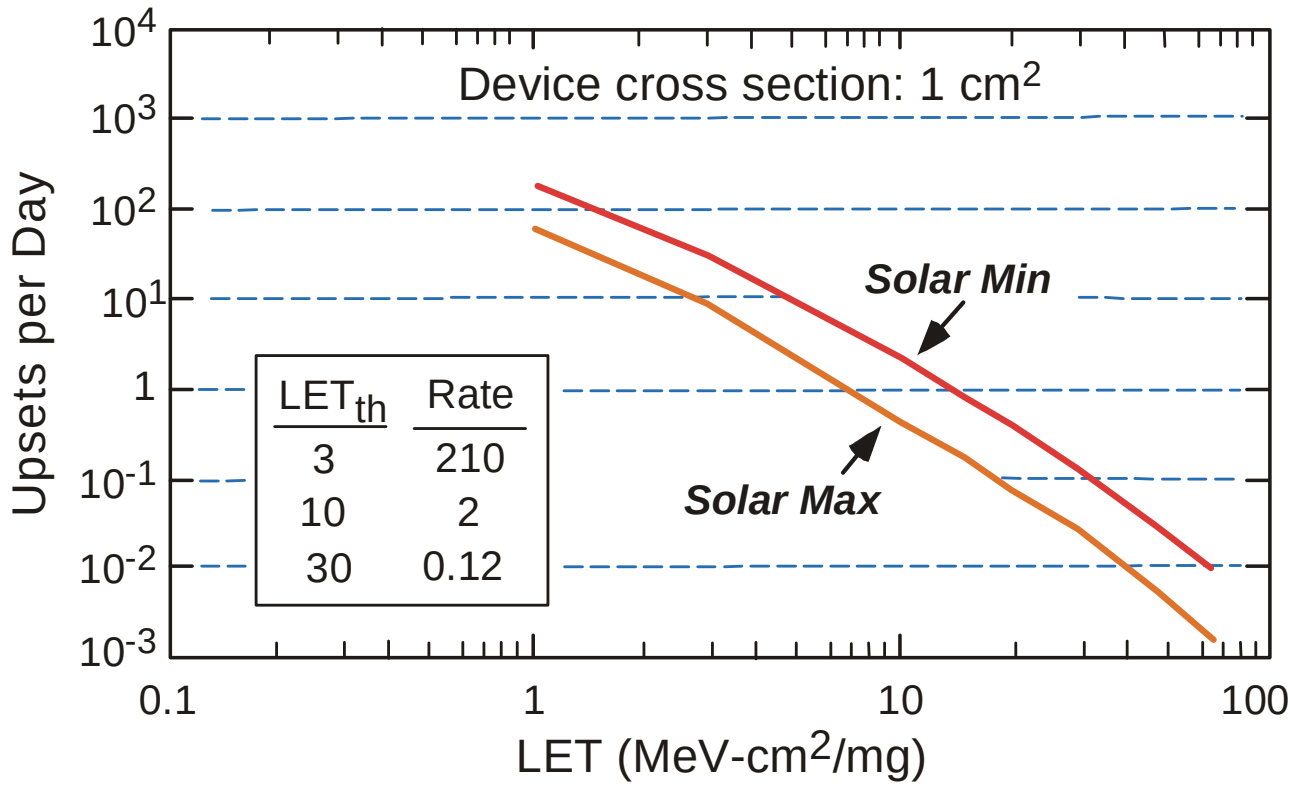
The CREME96 code (NRL) is one example of a code for rate calculations

Approximate Rate Estimations in Deep Space

The upset rate in this figure corresponds to a saturated cross section of 1 cm^2

We are assuming a step function for the cross section vs. LET curve in this example

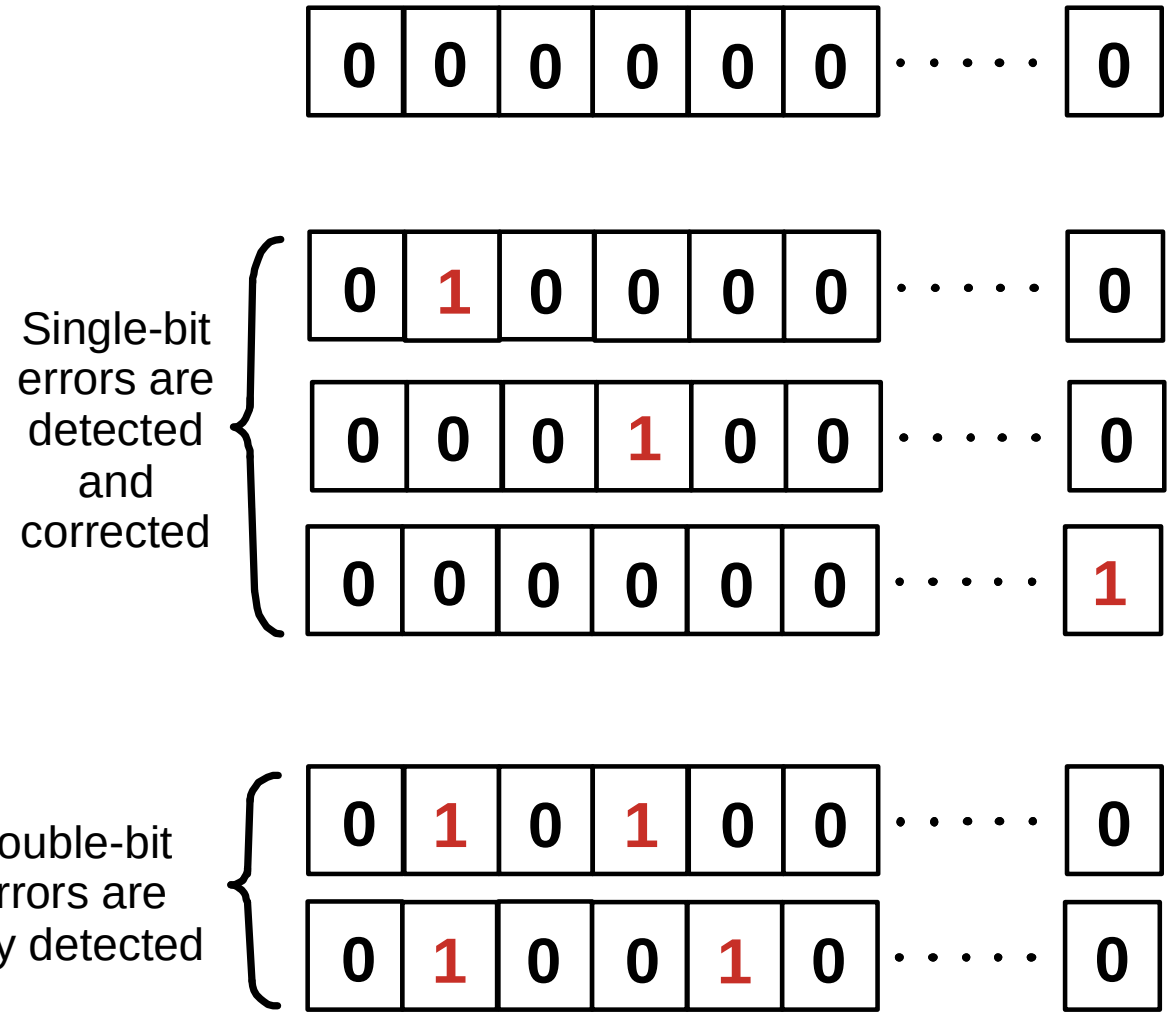
For a real device, multiply the rate per day by the measured saturation cross section



Error Detection and Correction

Adding 7 parity bits to a 32-bit word allows single-bit errors to be detected and corrected

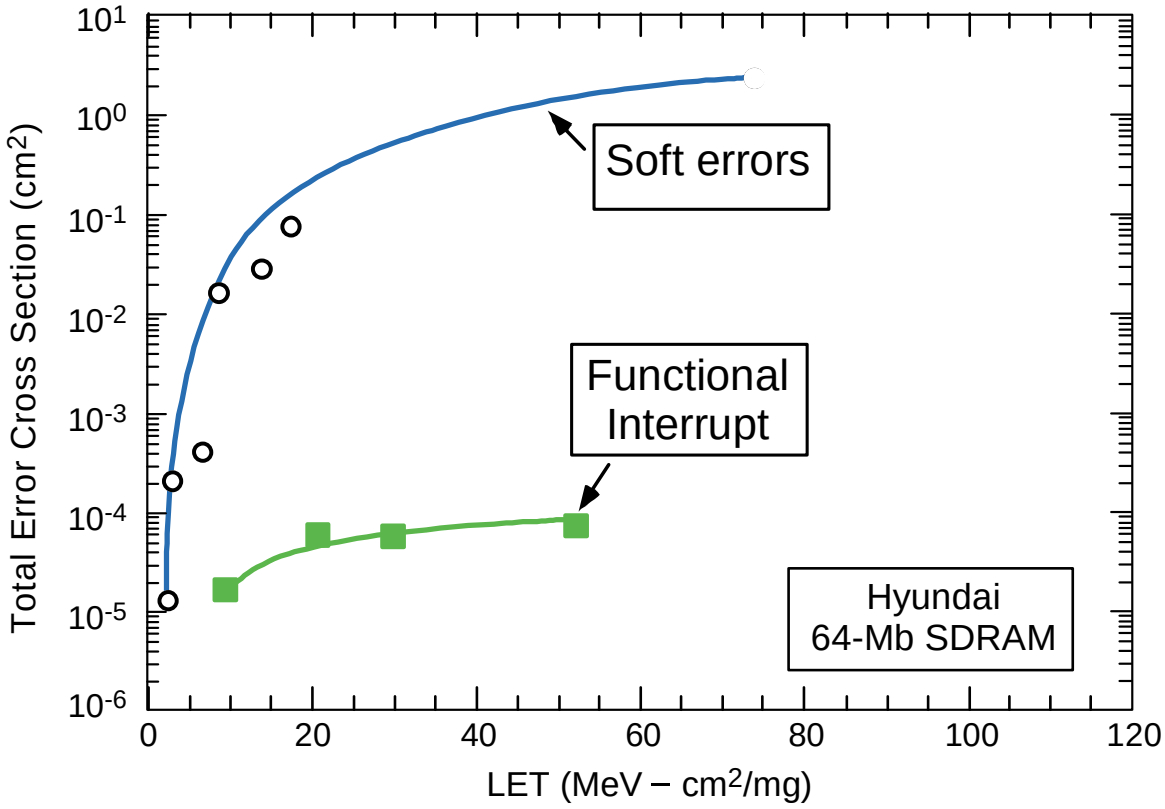
(Hamming Code)



Functional Interrupts in a More Advanced DRAM

Modern DRAMs are more complex, increasing the “SEFI” cross section to the point where it is only 1000X lower than the total cell upset rate

Detecting functional interrupts is a major issue for advanced DRAMs when they are used in space



Circuit Technologies where SEFI Is Important

Advanced Memories
- Internal test modes
- Micro-programmed cell architecture

Flash Memories
- Dominant effect
- “Crashes” internal state controller and buffers

Xilinx Programmable Logic Arrays

Microprocessors
- Many categories of responses
- Detection and recovery are very difficult problems
- “Crashes” and “Hangs” require restart

Microprocessors

- Microprocessors are highly sensitive to SEEs
  - Even Radiation Hardened devices can exhibit upsets
  - Threshold LET of commercial processors is ~ 2 MeV-cm^2/mg
- CACHE and Register Upsets (SRAM)
  - Corrupt data and instructions
  - Internal transients in high-speed logic
- Program can execute incorrectly, calculate something wrong, or hang the processor (may require “cold boot”)
- Microprocessors are very hard to test because not every SEE will result in an observable error
  - Application dependent

Mitigation

– Triple or more (in case of hangs) redundancy voting

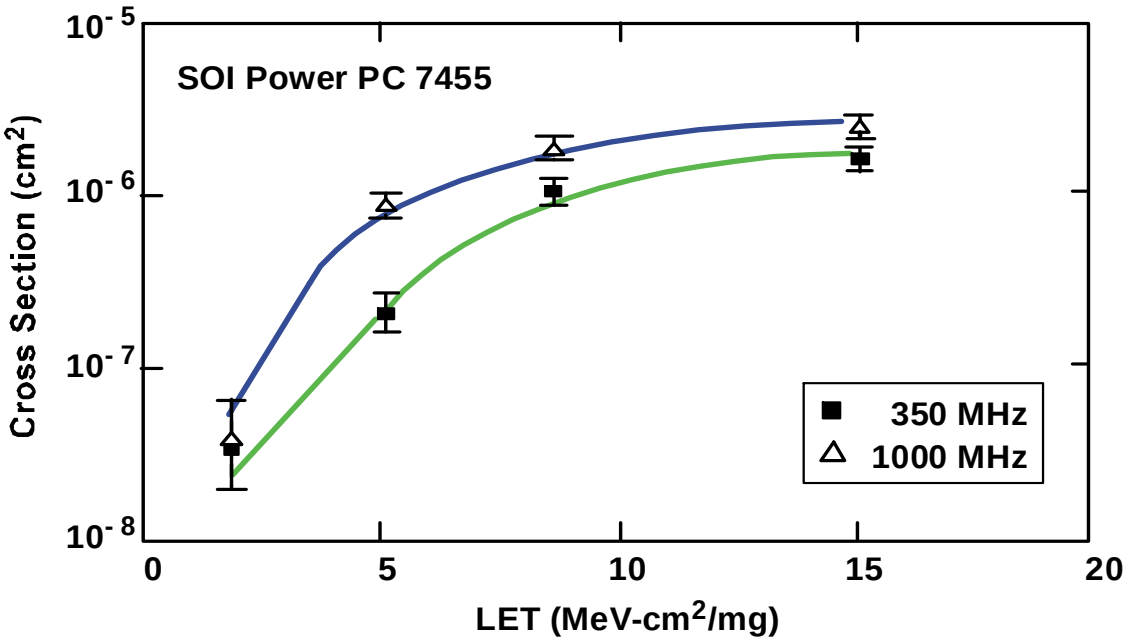
Continuing Issues for Computer Systems

Complex errors and “hangs” in processors

Errors in key components such as the bridge chip

Complex memory errors that may not be amenable to EDAC

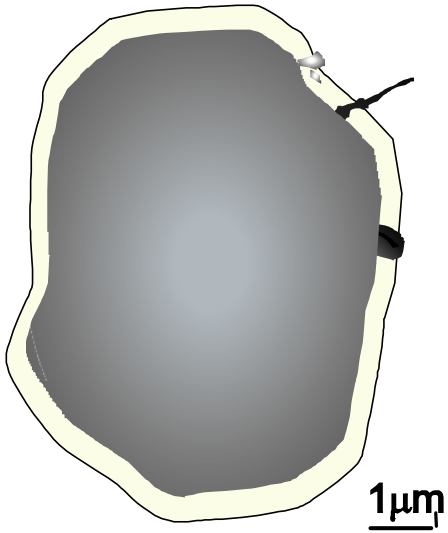
Increased error rate at high clock speed



F. Irom and F. Farmanesh, IEEE Trans. Nucl. Sci., **51**(3505), 2004.

Catastrophic SEU Effects

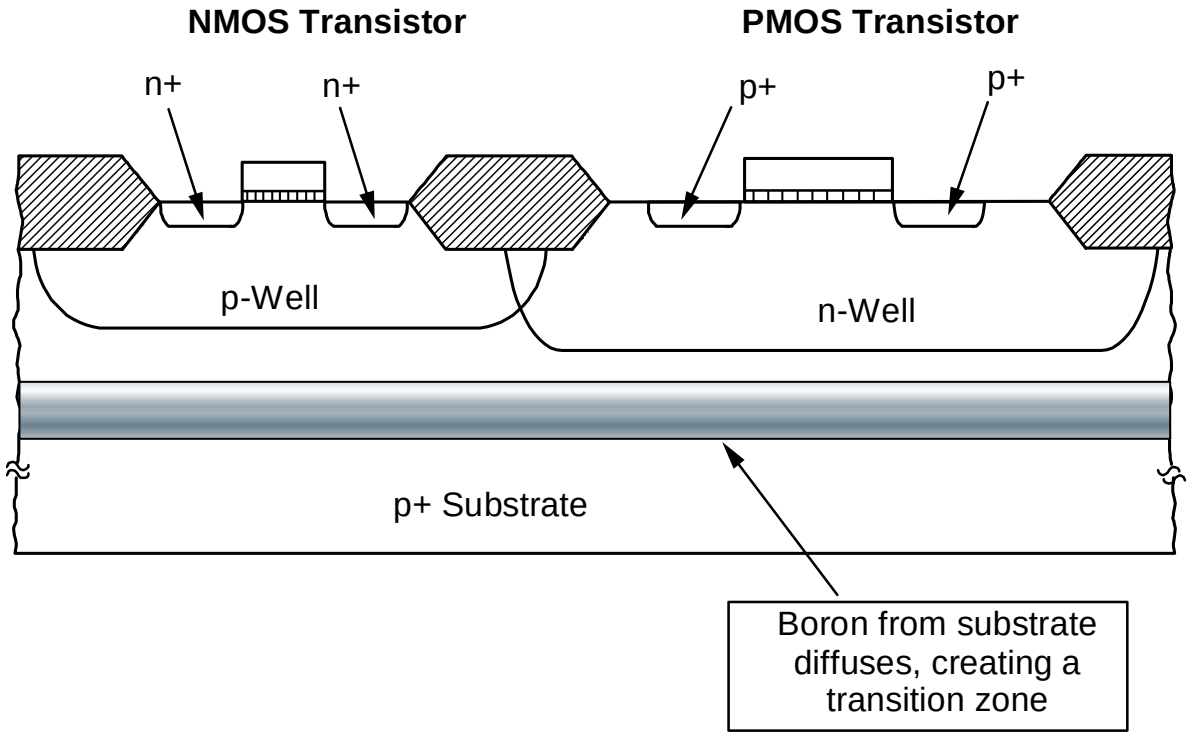
- Latchup in CMOS
- Gate rupture and breakdown in power devices



Basic CMOS Structure

Lateral isolation provided by field oxide (or trench, for newer devices)

Vertical isolation relies on reverse-biased p-n junctions



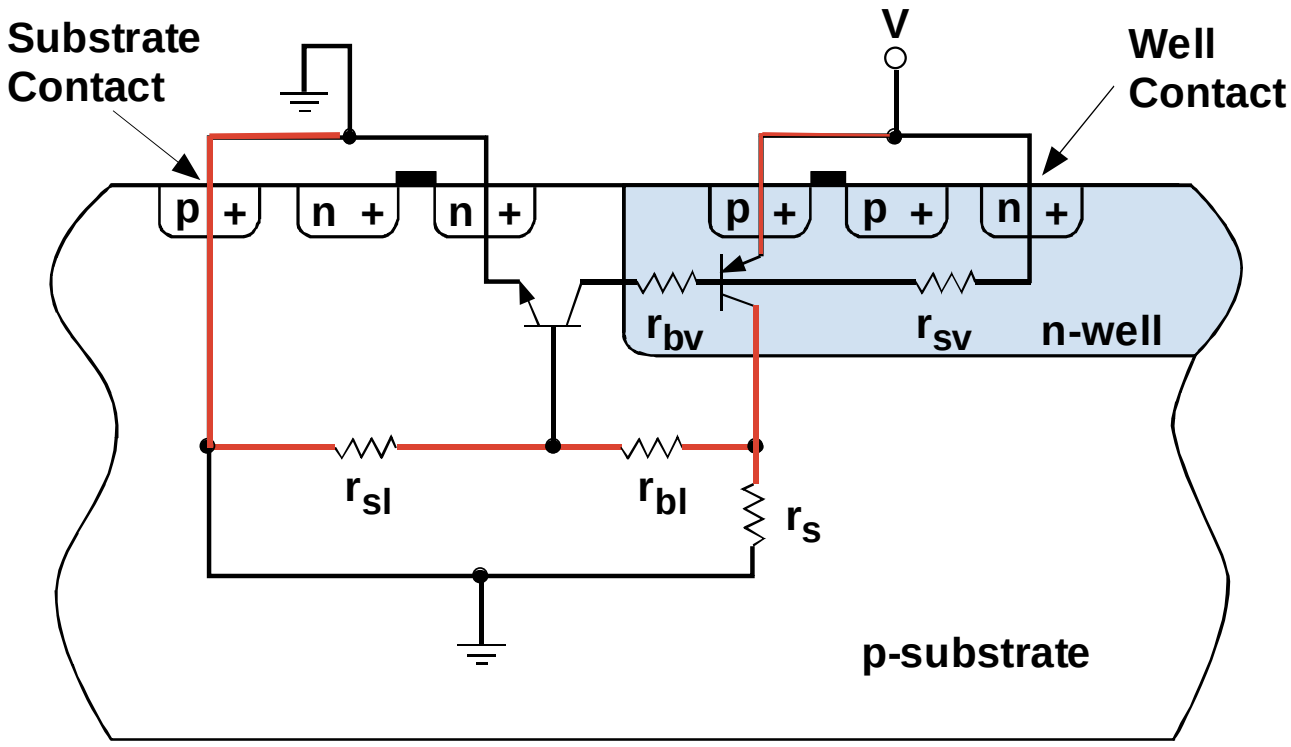
The parasitic p-n isolation junctions are responsible for latchup in CMOS

Single-Particle Latchup (triggered by ions in space)

Latchup creates a low-resistance path from power supply to ground

Current remains high until power is removed

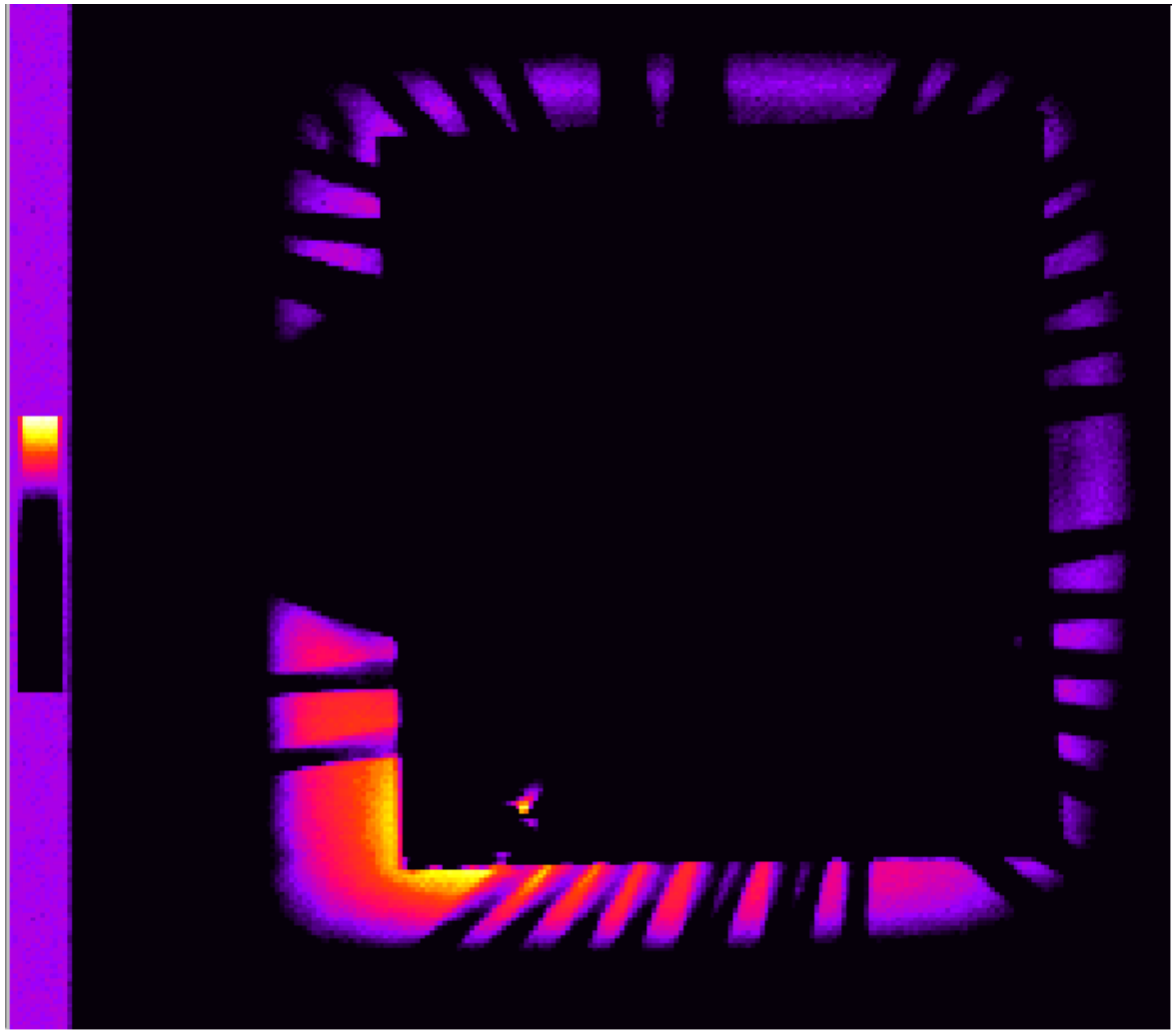
Current path is highly localized



Thermal Imaging of a CMOS Devices During Latchup

Yellow color shows regions with high temperature

Latchup current (several hundred mA) flows in the small region at the left corner



Consequences of Latchup

Three Possible Consequences:

- Instant, catastrophic device failure
  - Metallization vaporization
  - Contact or wire bond failure
  - Melting of underlying silicon
- Latent damage that affects reliability
  - Metallization re-crystallization and weakening of metal bonds
  - Ejection of vaporized metal creating localized voids
- Device returns to normal operation after a power cycle with no obvious internal damage

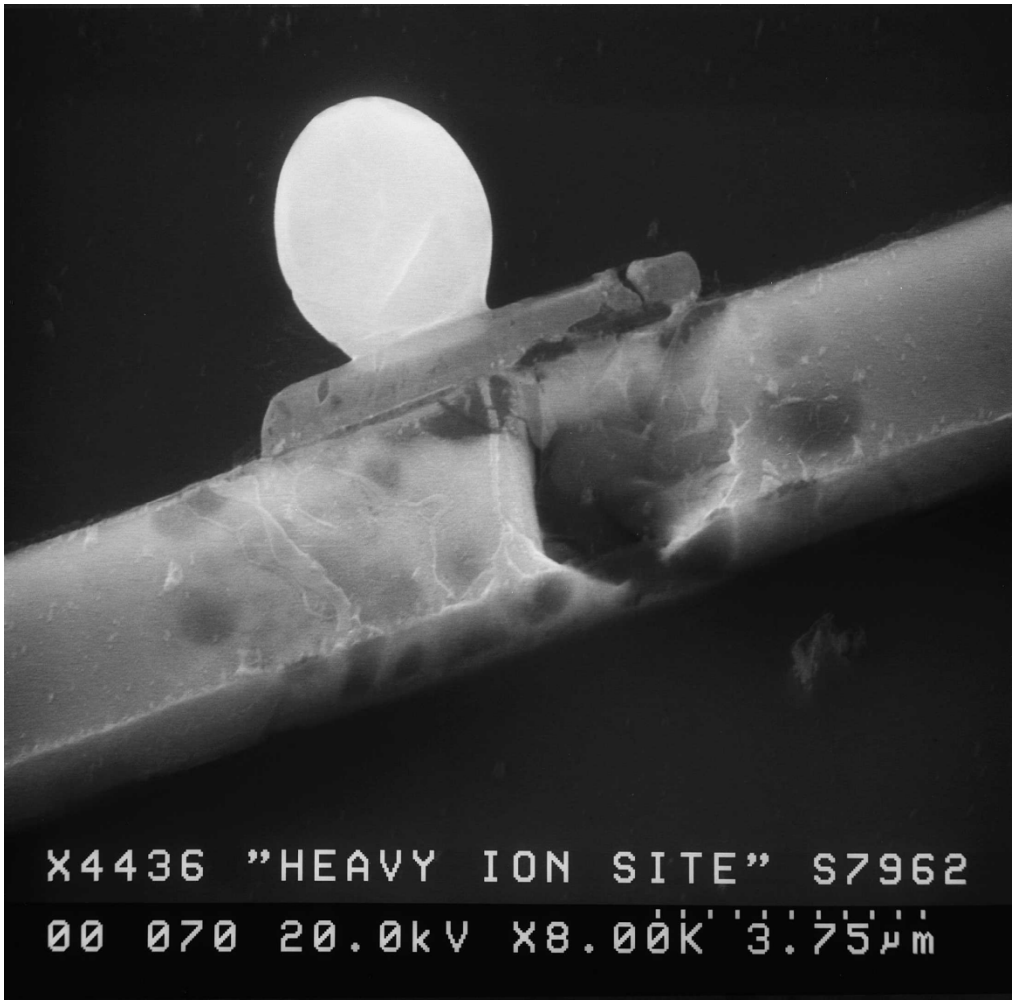
Many Modern Devices Are Susceptible to Catastrophic Damage

AD9240 Latent Damage

Melting occurred in a metal-1 trace during latchup

The trace was not designed to handle the higher current that takes place during a latchup event

In this example, metal was ejected, but the trace still conducted



H. Becker, *et al*, IEEE Trans. Nucl. Sci., **49**(3082), 2002.

Dealing with Latchup

All CMOS Devices (except SOI) Are Potentially Sensitive to Latchup

- Changes in fabrication technology can occur that change latchup characteristics
- In most cases radiation testing must be done for specific lots used on systems
- Radiation-hardened parts are usually acceptable without additional testing

Radiation Testing May Show that the Latchup Probability Is Low Enough for Mission Requirements

- Often the case when the LET threshold is ~ 50 MeV-cm^2/mg or more
- Latchup circumvention may be acceptable if very few events are anticipated during the mission
- Difficult and costly to validate circumvention methods

SEL Detection and Mitigation

Detection circuits can't detect all latchup events

- Need "headroom" for current fluctuations during normal operation
- There are many different internal latchup paths in most circuits, with different characteristics and current signatures

Current shutdown may not be fast enough

- Capacitors on circuit boards provide localized charge
- Latent damage can take place within a few microseconds

Practical limitations are imposed by

- Unit-to-unit variability in latchup current and operating current
- Effect of temperature and aging on device operation
- Temperature and LET sensitivity of latchup characteristics

Catastrophic Failure in Power Devices

Gate Rupture

Gate is destroyed by an ion strike near the gate edge

Effect is worse for normal incidence

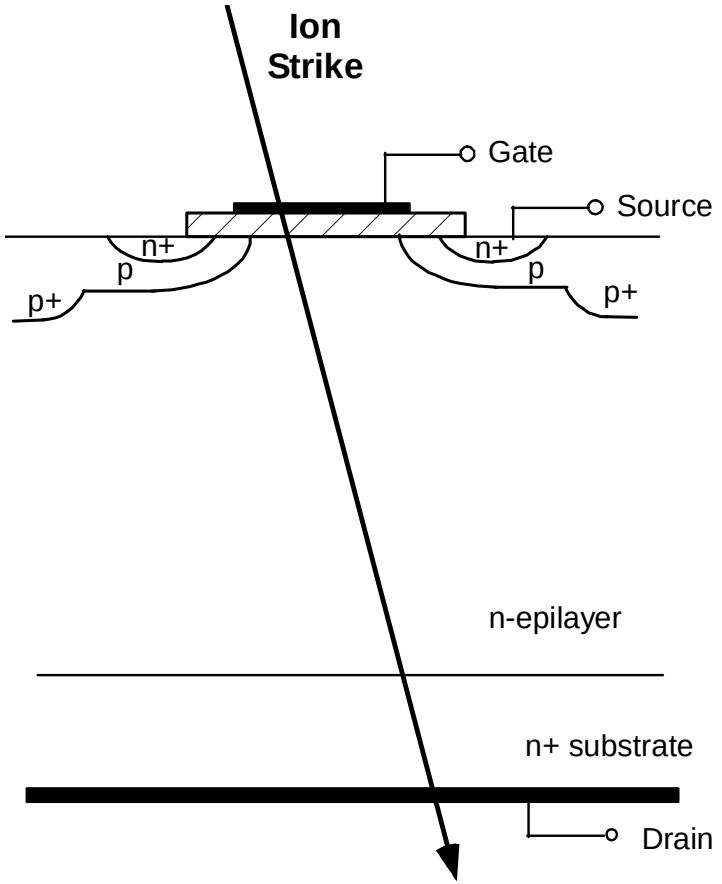
Very strong voltage dependence

- Gate voltage
- Supply voltage

Weak temperature dependence

Cross section is usually very abrupt

Large numbers of parts are required for testing

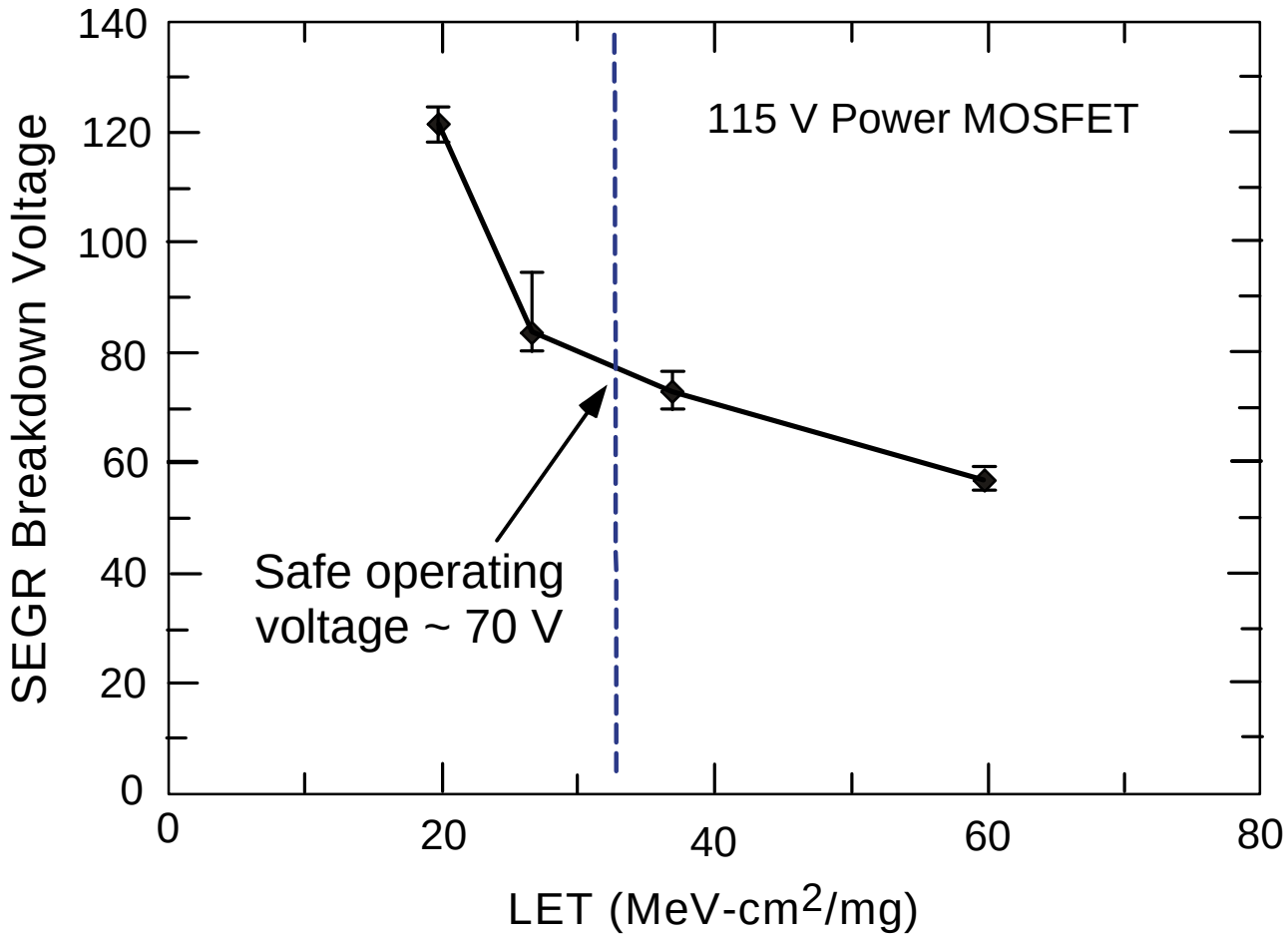


A similar mechanism, single-event burnout, occurs in bipolar power transistors.

Representative Test Results for a Moderate Voltage Power MOSFET

Gate rupture can be eliminated by operating the device at reduced voltage

Additional allowance must be made for unit-to-unit variability



Part De-rating Is Effective for SEGR and SEB

Usual practice is to reduce maximum drain voltage to 75% of drain voltage where parts are affected during testing

- E.g., if SEGR takes place at 140 V for “200 V part”, reduce maximum application voltage to 105 V
- Gate and drain voltage both affect results

Hardened power MOSFETs are available, and are recommended for most space applications

Devices with high voltage ratings are more susceptible, and require larger fractional derating

Summary

Hardened microelectronic devices are the preferred technologies for Europa because of the very high total dose requirement

- Some commercial technologies will be used as well
- The APML provides the best path for part selection
- Costs and other challenges make it difficult to test and qualify parts

Single-particle effects are similar to that of other missions

- They are still important, particularly because of the long mission duration
  - Complex functional responses are particularly difficult
  - Systems and circuits must be able to recover from their effects
- Catastrophic effects (latchup and SEGR/SEB) are the most important overall issues

Selected References

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- April, 1996
- June, 2003

Notes from IEEE Radiation Effects Short Courses, 1980 – 2007

Books

- T. P. Ma and P. V. Dressendorfer (Eds.), *Ionizing Radiation Effects in MOS Devices and Circuits*, Wiley, 1989.
- G. C. Messenger and M. S. Ash, *The Effects of Radiation on Electronic Systems*, Van Nostrand Rheinhold, 1992.
- G. C. Messenger and M. S. Ash, *Single Event Phenomena*, Chapman and Hall, 1997.

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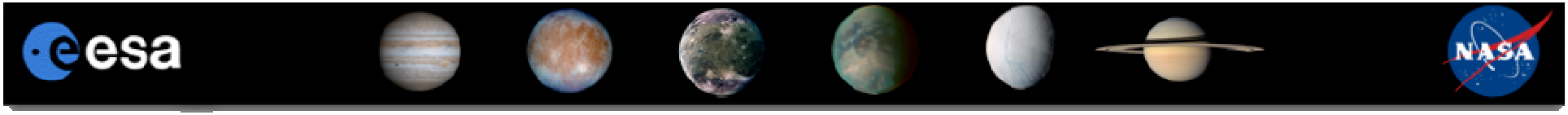

Questions & Answers